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PREFACE

The purpose of this Technical Manual is to explain and illustrate the hardware and software technical details of the Universal Serial Controller (USC),

The document is organized into six chapters and an Appendix as follows:

1. General Description

Chapter 1 is an introductory section covering the key features, overview block diagrams, pin-outs and pin definitions.

2. Interfacing the USC

Chapter 2 provides all of the technical information to describe the bus interfaces, bus transactions and register accesses.

3. Detailed Functional Descriptions

Chapter 3 covers the USC's functional details in the areas of receiver, transmitter, baud rate generator, digital phase lock loop, character counters, polling, interrupts, direct memory access, clock options, and data encoding/decoding.

4. Modes of Operation

Chapter 4 explains the asynchronous, bit- and byte-oriented synchronous modes along with mode selection.

5. Register Descriptions

Chapter 5 illustrates and explains all of the bit combinations and meanings of every USC register configuration.

6. Test Modes

Chapter 6 illustrates the various test mode registers that allow the user special access to internal registers for testing purposes.

The user can trace the data through the USC to debug and/or optimize his software.

7. Appendix A

Appendix A illustrates the 16-bit data configurations for the various asynchronous and synchronous modes.

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CHAPTER 1

GENERAL DESCRIPTION

1.1 INTRODUCTION

The USC Universal Serial Controller is a dual-channel, multi-protocol data communications peripheral designed for use with any conventional multiplexed or non-multiplexed bus. The USC functions as a serial-to-parallel, parallel-to-serial converter/controller and may be software configured to satisfy a wide variety of serial communica-

tions applications. The device contains a variety of new, sophisticated internal functions including two baud rate generators per channel, a digital phase-locked loop per channel, character counters for both receive and transmit in each channel and 32 byte data FIFO's for each receiver and transmitter (Figure 1-1).

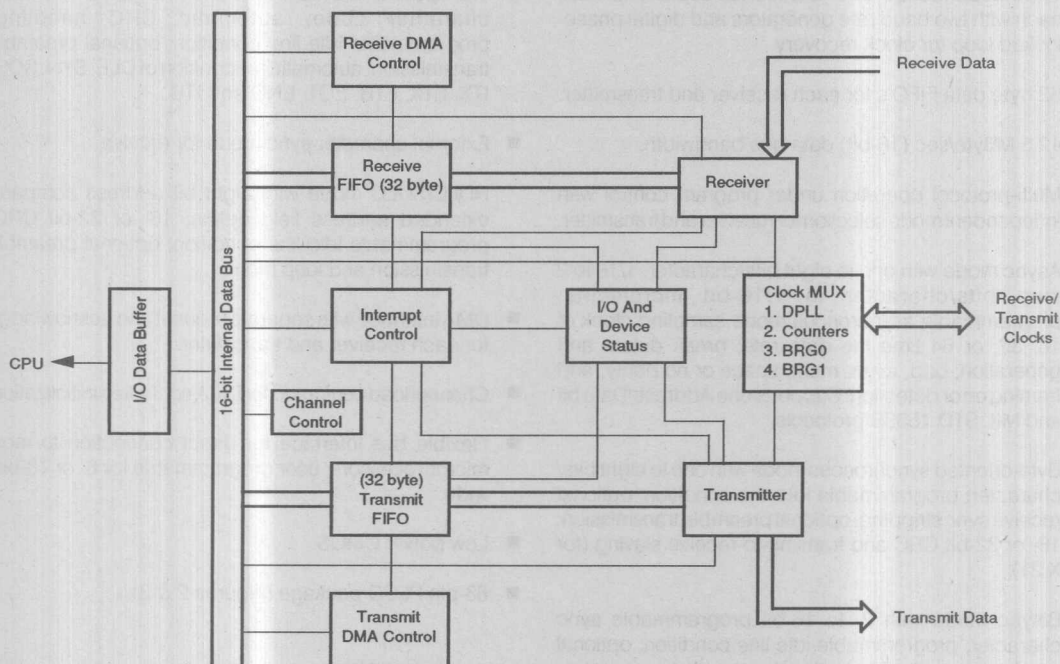


Figure 1-1. USC Block Diagram

The USC handles asynchronous formats, synchronous, byte-oriented formats such as BISYNC and synchronous bit-oriented formats such as HDLC. This device supports virtually any serial data transfer application.

The device can generate and check CRC in any synchronous mode and can be programmed to check data integrity in various modes. The USC also has facilities for modem controls in both channels. In applications where these controls are not needed, the modem controls may be used for general-purpose I/O. The same is true for most of the other pins in each channel.

Interrupts are supported with a daisy-chain hierarchy, with the two channels having completely separate interrupt structures.

High-speed data transfers via DMA are supported by a Request/Acknowledge signal pair for each receiver and transmitter. The device supports automatic status transfer via DMA and allows device initialization under DMA control also.

To aid the designer in efficiently programming the USC, support tools are available. The Programmer's Assistant is an MS-DOS disk-based programming initialization tool to be used in conjunction with the Technical Manual. There are also available assorted application notes and development boards to assist the designer in the hardware/software development.

1.2 FEATURES

- Two independent, 0 to 10Mbit/sec, full-duplex channels, each with two baud rate generators and digital phase-locked loop for clock recovery.
- 32 byte data FIFO's for each receiver and transmitter.
- 12.5 MByte/sec (16-bit) data bus bandwidth.
- Multi-protocol operation under program control with independent mode selection for receiver and transmitter.
- Async mode with one to eight bits/character, 1/16 to 2 stop bits/character in 1/16-bit increments; programmable asynchronous mode sampling clock of 16, 32, or 64 times the data rate; break detect and generation; odd, even, mark, space or no parity; and framing error detection. Supports one Address/Data bit and MIL STD 1553B protocols.
- Byte-oriented synchronous mode with one to eight bits/character; programmable idle line condition; optional receive sync stripping; optional preamble transmission; 16- or 32-bit CRC and transmit-to-receive slaving (for X.21).
- Bisync mode with 2- to 16-bit programmable sync character; programmable idle line condition; optional receive sync stripping; optional preamble transmission; 16- or 32-bit CRC.
- Transparent Bisync mode with EBCDIC or ASCII character code; automatic CRC handling; programmable idle line condition; optional preamble transmission; automatic recognition of DLE, SYN, SOH, ITX, ETX, ETB, EOT, ENQ and ITB.
- External character sync mode for receive.
- HDLC/SDLC mode with eight bit address compare; extended address field option; 16- or 32-bit CRC; programmable idle line condition; optional preamble transmission and loop mode.
- DMA interface with separate request and acknowledge for each receiver and transmitter.
- Channel load command for DMA controlled initialization.
- Flexible bus interface for direct connection to most microprocessors; user programmable for 8- or 16-bits wide.
- Low power CMOS.
- 68-pin PLCC package (Figures 2 & 3).

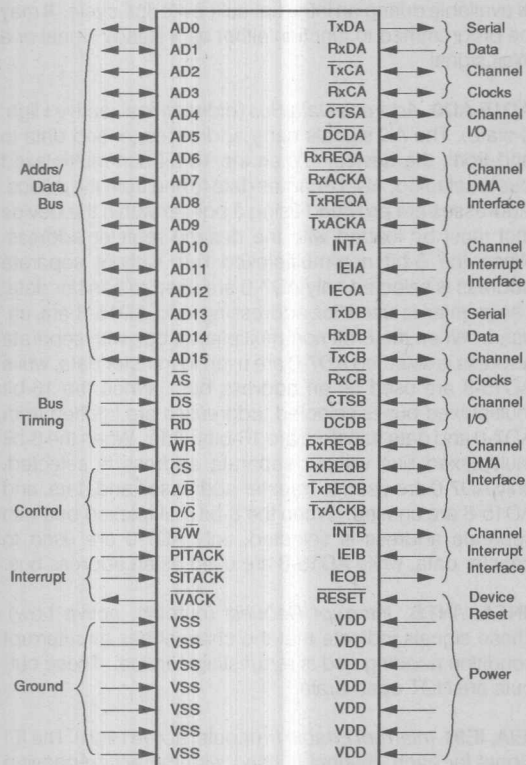


Figure 1-2. Pin Functions

1.3 PIN DESCRIPTION

The device contains thirteen pins per channel for channel I/O, sixteen pins for address and data, twelve pins for CPU handshake and fourteen pins for power and ground.

Three separate bus interface types are available for the device. The Bus Configuration Register (BCR) and external connections to the A/D bus control selection of the bus type.

A 16-bit bus is selected by setting BCR bit 2 to a 1.

The eight bit bus is selected by setting BCR bit 2 to zero and tying AD15 - AD8 to Vss.

The eight bit bus with separate address is selected by setting BCR bit 2 to zero and,

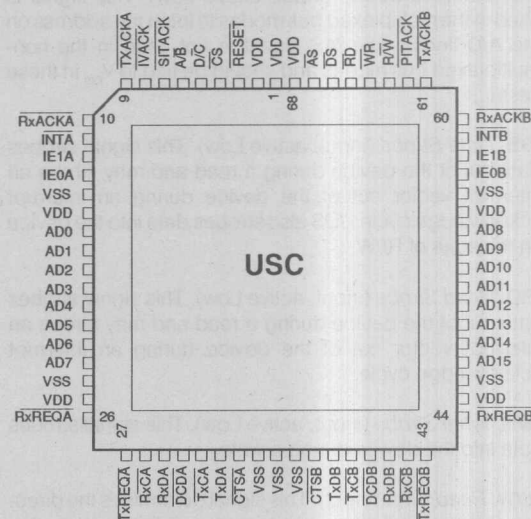


Figure 1-3. Pin Assignments

during the BCR write, forcing AD15 to a 1 and forcing AD14-AD8 to zero.

The multiplexed bus is selected for the USC if there is an Address Strobe prior to or during the transaction which writes the BCR. If no Address Strobe is present prior to or during the transaction which writes the BCR, a multiplexed bus is selected.

The section below describes in detail the USC pin assignment.

/RESET. *Reset* (input, active Low). This signal resets the device to a known state. The first write to the USC after a reset accesses the BCR to select additional bus options for the device.

/AS. Address Strobe (input, active Low). This signal is used in the multiplexed bus modes to latch the address on the A/D lines. The /AS signal is not used in the non-multiplexed bus modes and should be tied to V_{DD} in these cases.

/DS. Data Strobe (input, active Low). This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle. /DS also strobes data into the device on the state of R/W.

/RD. Read Strobe (input, active Low). This signal strobes data out of the device during a read and may strobe an interrupt vector out of the device during an interrupt acknowledge cycle.

/WR. Write Strobe (input, active Low). This signal strobes data into the device during a write.

R/W. Read/Write (input). This signal determines the direction of data transfer for a read or write cycle in conjunction with /DS.

/CS. Chip Select (input, active Low). This signal selects the device for access and must be asserted for read and write cycles, but is ignored during interrupt acknowledge and fly-by DMA transfers. In the case of a multiplexed bus interface, /CS is latched by the rising edge of /AS.

A/B. Channel A/Channel B Select (input). This signal selects between the two channels in the device. High selects channel A and Low selects channel B.

D/C. Data/Control Select (input). This signal, when High, provides for direct access to the RDR and TDR. In the case of a multiplexed bus interface, D/C High overrides the address provided to the device.

/SITACK. Status Interrupt Acknowledge (input, active Low). This signal is a status signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle.

/PITACK. Pulsed Interrupt Acknowledge (input, active Low). This signal is a strobe signal that indicates that an interrupt acknowledge cycle is in progress. The device is capable of returning an interrupt vector that may be encoded with the type of interrupt pending during this acknowledge cycle.

/IVACK. Interrupt Vector Acknowledge/Wait (output, active Low). This signal serves to indicate when a valid vector

is available during an interrupt acknowledge cycle. It may be programmed to function either as a Ready signal or a Wait signal.

AD15-AD0. Address/Data Bus (bidirectional, active High, 3-state). The AD signals carry addresses to, and data to and from, the device. When the 16-bit non-multiplexed bus is selected, AD-15 carries data to and from the device. Addresses are provided using a pointer within the device that must be loaded with the desired register address. When the 8-bit non-multiplexed bus without separate address is selected only AD7-0 are used to transfer data. The pointer is used for addressing and AD15-8 are unused. When the 8-bit non-multiplexed bus with separate address is selected AD7-0 are used to transfer data, while AD15-8 are used as an address bus. When the 16-bit multiplexed bus is selected, addresses are latched from AD7-0 and data transfers are 16-bits wide. When the 8-bit multiplexed bus without separate address is selected, only AD7-0 are used to transfer addresses and data, and AD15-8 are unused. When the 8-bit multiplexed bus with separate address is selected, only AD7-0 are used to transfer data, while AD15-8 are used as an address bus.

/INTA, /INTB. Interrupt Request (outputs, active Low). These signals indicate that the channel has an interrupt condition pending and is requesting service. These outputs are NOT open-drain.

IEIA, IEIB. Interrupt Enable In (inputs, active High). The IEI signal for each channel is used with the accompanying IEO signal to form an interrupt daisy chain. An active IEI indicates that no device having higher priority is requesting or servicing an interrupt.

IEOA, IEOB. Interrupt Enable Out (outputs, active High). The IEO signal for each channel is used with the accompanying IEI signal to form an interrupt daisy chain. IEO is Low if IEI is Low, an interrupt is under service in the channel, or an interrupt is pending during an interrupt acknowledge cycle.

/TXACKA, /TXACKB. Transmit Acknowledge (inputs or outputs, active low). The primary function of these signals is to perform fly-by DMA transfers to the transmit FIFOs. They may also be used as bit inputs or outputs.

/RXACKA, /RXACKB. Receive Acknowledge (inputs or outputs, active Low). The primary function of these signals is to perform fly-by DMA transfers from the receive FIFOs. They may also be used as bit inputs or outputs.

TXDA, TXDB. Transmit Data (outputs, active High, 3-state). These signals carry the serial transmit data for each channel.

RXDA, RXDB. *Receive Data* (inputs, active High). These signals carry the serial receive data for each channel.

/TXCA, /TXCB. *Transmit Clock* (inputs or outputs, active Low). These signals may be used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various transmitter signals or internal clock signals.

/RXCA, /RXCB. *Receive Clock* (inputs or outputs, active Low). These signals may be used as clock inputs for any of the functional blocks within the device. They may also be used as outputs for various receiver signals or internal clock signals.

/TXREQA, /TXREQB. *Transmit Request* (inputs or outputs, active Low). The primary function of these signals is to request DMA transfers to the transmit FIFOs. They may also be used as simple inputs or outputs.

/RXREQA, /RXREQB. *Receive Request* (inputs or outputs, active low). The primary function of these signals is to request DMA transfers from the receive FIFOs. They may also be used as simple inputs or outputs.

/CTSA, /CTSB. *Clear To Send* (inputs or outputs, active Low). These signals may be used as enables for the respective transmitters. They may also be programmed to generate interrupts on either transition or used as simple inputs or outputs.

/DCDA, /DCDB. *Data Carrier Detect* (inputs or outputs, active Low). These signals may be used as enables for the respective receivers. They may also be programmed to generate interrupts on either transition or used as simple inputs or outputs.



AUGUST 1989

2.1 INTRODUCTION

This chapter describes the details of interfacing the USC to a system. The general timing requirements for the USC are described, but the data sheet must be referenced for specific AC numbers.

2.2 USC BUS INTERFACE

The USC is unique in that the bus interface for the device provides the resources necessary to interface the USC to virtually any type of bus. The USC directly supports either a 16-bit bus or an 8-bit bus, but may be easily connected to a 32-bit bus as well. The control signals provided allow connection to either a multiplexed address/data type bus or to a separate address and data type bus. Interrupt acknowledge may be signaled either through a status line or via a dedicated interrupt acknowledge strobe signal. In addition, fly-by DMA transfers are supported for both receive and transmit.

It is important to note that the USC does not have a clock input. In this regard the USC "looks" like a memory rather than a traditional peripheral device. All bus timing information is carried in the control signals for the bus and interrupt, and DMA requests are generated asynchronously.

The six different general bus types are described below, with the specific bus transactions described in the following section.

2.2.1 Multiplexed 16-Bit Bus

In this case, AD15-0 carry addresses to the USC and 16-bit data to and from the USC. The addresses on AD7-0 are latched into the USC on the rising edge of the /AS signal, along with the chip select (/CS) and potentially the Interrupt Acknowledge status on the /SITACK signal. Because the register address is latched on every bus transaction, all of the registers in the USC are directly accessible. This bus interface provides the highest bus bandwidth capability

CHAPTER 2

INTERFACING THE USC.

for the USC. Figures 2-1 through 2-9 show the multiplexed bus timing diagrams.

2.2.2 Non-multiplexed 16-Bit Bus

In this case, AD15-0 carry 16-bit data to and from the USC. Only the receive and transmit data registers and the Channel Command/Address Register (CCAR) are directly accessible, with all other registers being accessed by first writing a register address to the CCAR and then accessing the desired register. This bus interface provides the same high bus bandwidth as the multiplexed 16-bit bus when accessing either the transmit or receive data registers because these registers may still be accessed directly in this case using the D//C signal, or via fly-by DMA transfers using /TXACK or /RXACK. Figures 2-10 through 2-18 show the non-multiplexed bus timing diagrams.

2.2.3 Multiplexed 8-Bit Bus

In this case, AD7-0 carry addresses to the USC and 8-bit data to and from the USC. AD15-8 is not used. The addresses on AD7-0 are latched into the USC on the rising edge of the /AS signal, along with the chip select (/CS), and potentially the Interrupt Acknowledge status on the /SITACK signal. Because the register address is latched on every bus transaction, all of the registers in the USC are directly accessible, though only eight bits at a time. Fly-by DMA transfers are also 8-bits in this case.

2.2.4 Non-multiplexed 8 Bit Bus

In this case, AD7-0 carry 8-bit data to and from the USC and AD15-8 are unused. Only the receive and transmit data registers and the Channel Command/Address Register (CCAR) are directly accessible, with all other registers being accessed by first writing a register address to the CCAR and then accessing the desired register. The transmit and receive data registers may still be accessed directly in this case using the D//C signal, or via fly-by DMA transfers using /TXACK or /RXACK, though only eight bits at a time.

2.2.5 Separate Latched Address 8-Bit Bus

In this case, AD7-0 carry 8-bit data to and from the USC and AD15-8 are used to carry register addresses to the USC. The addresses on AD7-0 are latched into the USC on the rising edge of the /AS signal, along with the chip select (/CS), and potentially the Interrupt Acknowledge status on the /SITACK signal. Because the register address is latched on every bus transaction, all of the registers in the USC are directly accessible, though only eight bits at a time. Fly-by DMA transfers are also 8-bits in this case.

2.2.6 Separate Address 8-Bit Bus

In this case AD7-0 carry 8-bit data to and from the USC and AD15-8 are used to carry register addresses to the USC. The addresses on AD15-8 are latched into the USC on the falling edge of the strobe signal which transfers the data, along with the chip select (/CS), and potentially the Interrupt Acknowledge status on the /SITACK signal. Because the register address is latched on every bus transaction, all of the registers in the USC are directly accessible, though only eight bits at a time. Fly-by DMA transfers are also 8-bits in this case.

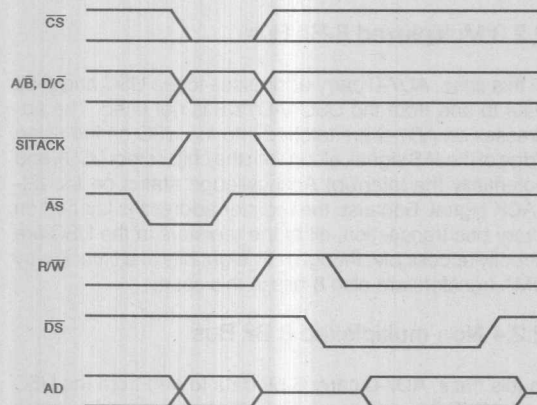


Figure 2-1. Multiplexed /DS Read Cycle

2.3 USC BUS TRANSACTIONS

This section will describe the different types of USC bus transactions in a general sense, for example, without the specific differences between an 8-bit bus and a 16-bit bus.

2.3.1 Multiplexed Read Transactions

The two possibilities for read transactions in a multiplexed bus are shown in Figures 2-1 and 2-2. The only difference between the two cases is the strobe used to transfer the data out of the USC. In Figure 2-1, the /DS signal, along with R/W selecting a read, strobes the data out of the USC, while in Figure 2-2 the /RD signal strobes the data out of the USC. In both cases, the register address is latched by the rising edge of the /AS signal, along with an active /CS and an inactive /SITACK signal.

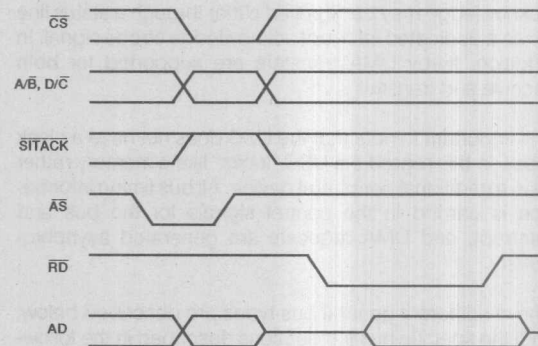


Figure 2-2. Multiplexed /RD Read Cycle

2.3.2 Multiplexed Write Transactions

The two possibilities for write transactions in a multiplexed bus are shown in Figures 2-3 and 2-4. The only difference between the two cases is the strobe used to transfer the data into the USC. In Figure 2-3, the /DS signal, along with R/W selecting a write, strobes the data into the USC while

in Figure 2-4 the /WR signal strobes the data into the USC. In both cases the register address is latched by the rising edge of the /AS signal, along with an active /CS and an inactive /SITACK signal.

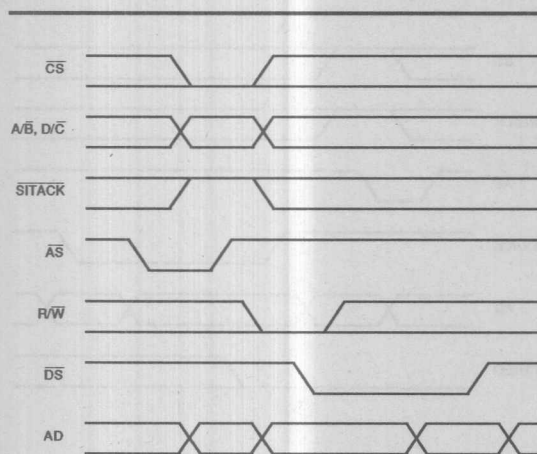


Figure 2-3. Multiplexed /DS Write Cycle

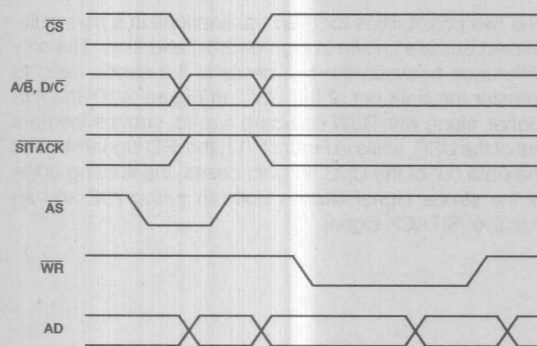


Figure 2-4. Multiplexed /WR Write Cycle

2.3.3 Multiplexed Interrupt Acknowledge Transactions

The three possibilities for interrupt acknowledge transactions in a multiplexed bus are shown in Figures 2-5, 2-6 and 2-7. The only difference between the first two is the strobe used to transfer the vector from the USC. In Figure 2-5 the /DS signal reads the vector out of the USC and sets the IUS bit in the interrupt section, while in Figure 2-6, the /RD signal performs this function. In Figure 2-7 the dedicated interrupt acknowledge strobe signal, /PITACK, is used to perform these functions. In these figures /IVACK is shown as a Ready signal. For /IVACK operation as a Wait signal refer to Figure 2-20.

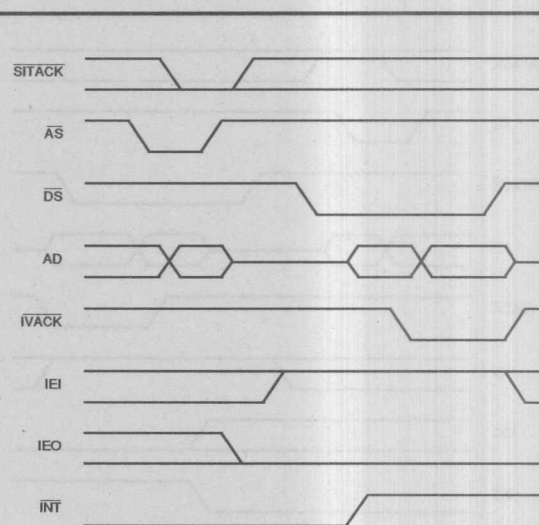


Figure 2-5. Multiplexed /DS Interrupt Acknowledge Cycle

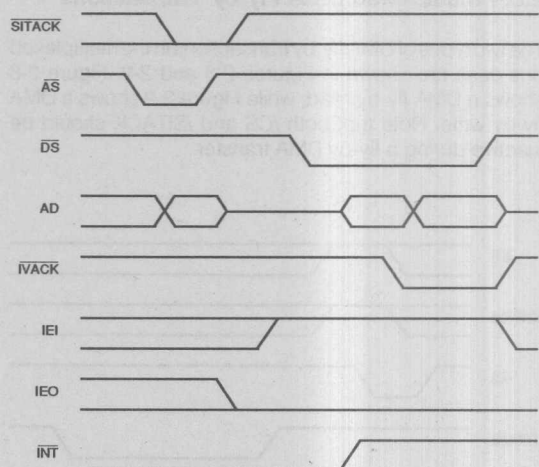


Figure 2-6. Multiplexed /RD Interrupt Acknowledge Cycle

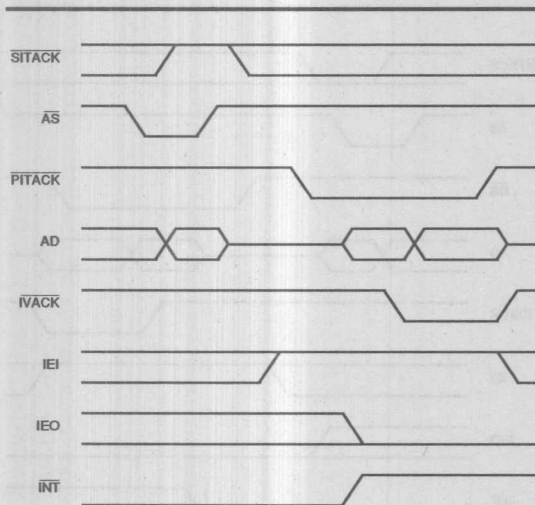


Figure 2-7. Multiplexed /PITACK Interrupt Acknowledge Cycle

2.3.4 Multiplexed DMA Fly-by Transactions

The two types of DMA fly-by transactions in the multiplexed bus case are shown in Figures 2-8 and 2-9. Figure 2-8 shows a DMA fly-by read, while Figure 2-9 shows a DMA fly-by write. Note that both /CS and /SITACK should be inactive during a fly-by DMA transfer.

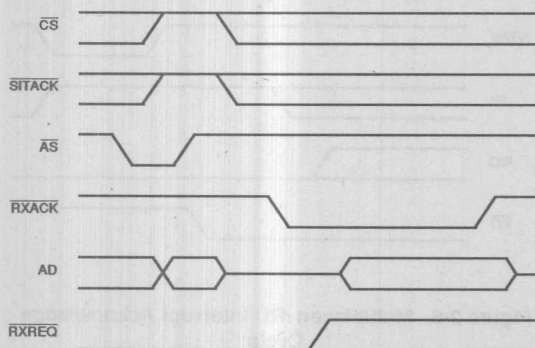


Figure 2-8. Multiplexed DMA Read Cycle

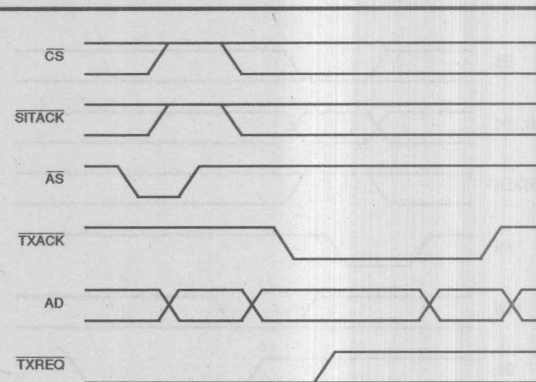


Figure 2-9. Multiplexed DMA Write Cycle

2.3.5 Non-multiplexed Read Transactions

The two possibilities for read transactions in a non-multiplexed bus are shown in Figures 2-10 and 2-11. The only difference between the two cases is the strobe used to transfer the data out of the USC. In Figure 2-10, the /DS signal, along with R/W selecting a read, strobes the data out of the USC, while in Figure 2-11, the /RD signal strobes the data out of the USC. In both cases, the leading edge of the strobe signal latches both an active /CS and an inactive /SITACK signal.

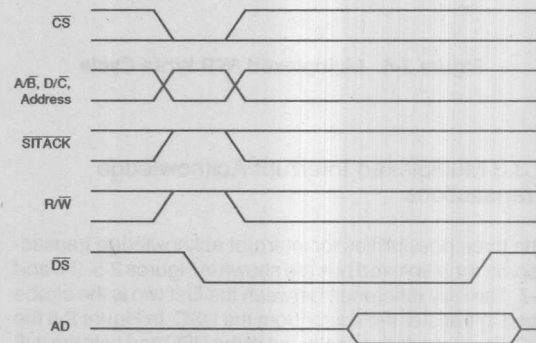


Figure 2-10. Non-Multiplexed /DS Read Cycle

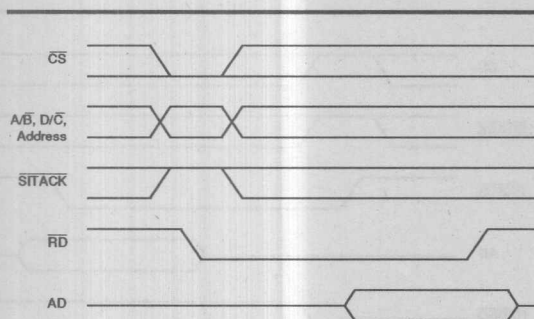


Figure 2-11. Non-Multiplexed /RD Read Cycle

2.3.6 Non-multiplexed Write Transactions

The two possibilities for write transactions in a multiplexed bus are shown in Figures 2-12 and 2-13. The only difference between the two cases is the strobe used to transfer the data into the USC. In Figure 2-12, the /DS signal, along with R/W selecting a write, strobes the data into the USC, while in Figure 2-13, the /WR signal strobes the data into the USC. In both cases, the leading edge of the strobe signal latches both an active /CS and an inactive /SITACK signal.

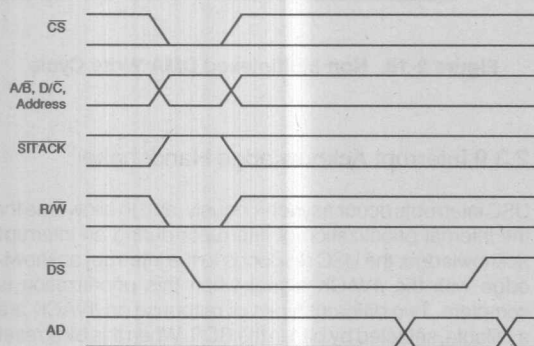


Figure 2-12. Non-Multiplexed /DS Write Cycle

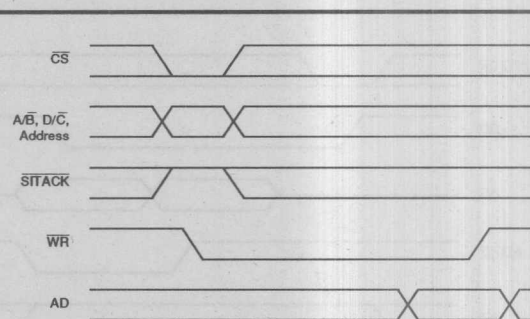


Figure 2-13. Non-Multiplexed /WR Write Cycle

2.3.7 Non-multiplexed Interrupt Acknowledge Transactions

The three possibilities for interrupt acknowledge transactions in a non-multiplexed bus are shown in Figures 2-14, 2-15 and 2-16. The only difference between the first two is the strobe used to transfer the vector from the USC. In Figure 2-14, the /DS signal reads the vector out of the USC and sets the IUS bit in the interrupt section, while in Figure 2-15, the /RD signal performs this function. In Figure 2-16, the dedicated interrupt acknowledge strobe signal, /PI-TACK, is used to perform these functions. In these figures, /IVACK is shown as a Ready signal. For /IVACK operation as a Wait signal refer to Figure 2-20.

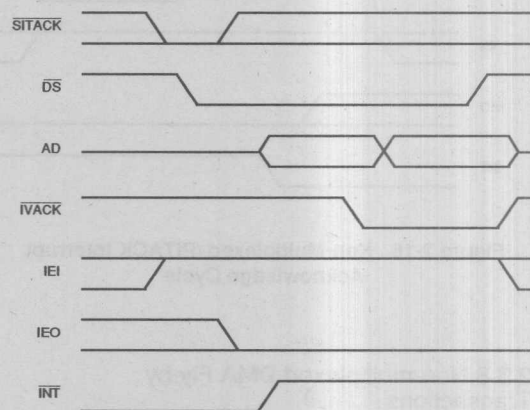


Figure 2-14. Non-Multiplexed /DS Interrupt Acknowledge Cycle

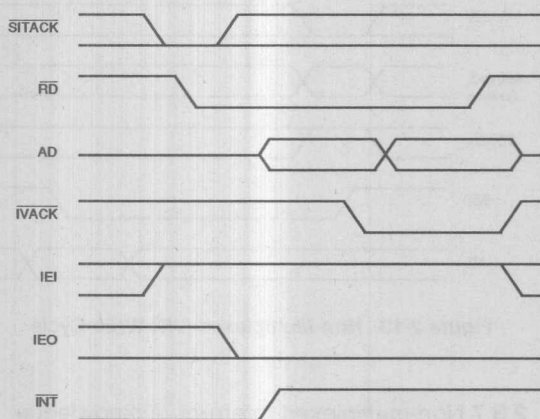


Figure 2-15. Non-Multiplexed /RD Interrupt Acknowledge Cycle

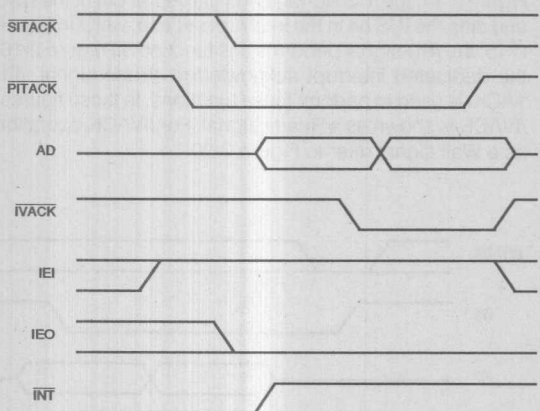


Figure 2-16. Non-Multiplexed /PITACK Interrupt Acknowledge Cycle

2.3.8 Non-multiplexed DMA Fly-by Transactions

The two types of DMA fly-by transactions are shown in Figures 2-17 and 2-18. Figure 2-17 shows a DMA fly-by read, while Figure 2-18 shows a DMA fly-by write. Note that both /CS and /SITACK should be inactive during a fly-by DMA transfer.

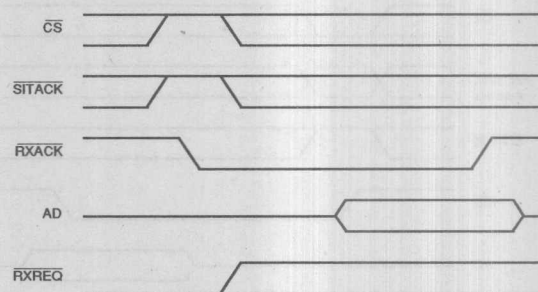


Figure 2-17. Non-Multiplexed DMA Read Cycle

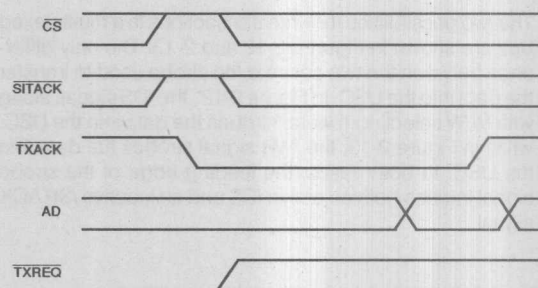


Figure 2-18. Non-Multiplexed DMA Write Cycle

2.3.9 Interrupt Acknowledge Handshake

USC interrupts occur asynchronously, and to allow time for the internal prioritization of interrupts during an interrupt acknowledge, the USC responds to the interrupt acknowledge with the /IVACK signal when this prioritization is complete. Two different types of response on /IVACK are available, selected by bit 1 in the BCR. When this bit is reset to 0, the /IVACK signal operates as a /Ready signal, as shown in Figure 2-19. When this bit is set to 1, the /IVACK signal operates as a /Wait signal as shown in Figure 2-20.

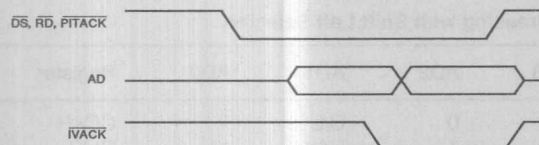


Figure 2-19. Interrupt Acknowledge Cycle with Ready

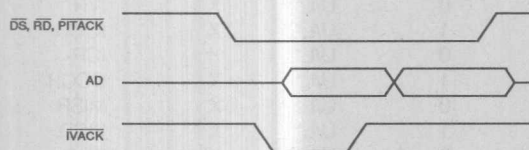


Figure 2-20. Interrupt Acknowledge Cycle with Wait

2.4 REGISTER ACCESS

USC registers may be accessed explicitly, directly, or indirectly, depending on the bus type and the specific control signals used. In all cases the B//W signal selects between a byte access (B//W High) and a word access (B//W Low). When an 8-bit bus is selected the B//W signal is always internally forced to 1, selecting a byte access. The U//L signal chooses between the upper byte (U//L High) and the lower byte (U//L Low) in the case of a byte access. U//L must always be Low for a word access.

Explicit addressing occurs only for three registers in the USC; These are the BCR, for the first write after a hardware reset; the RDR, either via a read with the D//C signal High, or by a fly-by DMA read; and the TDR, either by a write with the D//C signal High, or by a fly-by DMA write.

In the non-multiplexed bus case, only the CCAR is accessed directly, while in the multiplexed bus case all USC registers may be accessed directly. Likewise, when a separate address bus is used, all registers are directly addressed. There are two options available for address decoding in the multiplexed bus case, as shown in Tables 2.1 and 2.2. The address may be decoded from either A6-A0 (Shift Right) or A7-A1 (Shift Left). The selection of the decoding method is controlled by bit 0 in the BCR. The address decoding for the separate address bus case is shown in Table 2-3.

Table 2-1. Multiplexed Bus Addressing with Shift Left Selected

AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	Register
B/W*	0	0	0	0	0	U/L*	X	CCAR
B/W*	0	0	0	0	1	U/L*	X	CMR
B/W*	0	0	0	1	0	U/L*	X	CCSR
B/W*	0	0	0	1	1	U/L*	X	CCR
B/W*	0	0	1	0	0	U/L*	X	Reserved
B/W*	0	0	1	0	1	U/L*	X	Reserved
B/W*	0	0	1	1	0	U/L*	X	TMDR
B/W*	0	0	1	1	1	U/L*	X	TMCR
B/W*	0	1	0	0	0	U/L*	X	CMCR
B/W*	0	1	0	0	1	U/L*	X	HCR
B/W*	0	1	0	1	0	U/L*	X	IVR
B/W*	0	1	0	1	1	U/L*	X	IOCR
B/W*	0	1	1	0	0	U/L*	X	ICR
B/W*	0	1	1	0	1	U/L*	X	DCCR
B/W*	0	1	1	1	0	U/L*	X	MISR
B/W*	0	1	1	1	1	U/L*	X	SICR
B/W*	1	0	0	0	0	U/L*	X	RDR
B/W*	1	0	0	0	1	U/L*	X	RMR
B/W*	1	0	0	1	0	U/L*	X	RCSR
B/W*	1	0	0	1	1	U/L*	X	RICR
B/W*	1	0	1	0	0	U/L*	X	RSR
B/W*	1	0	1	0	1	U/L*	X	RCLR
B/W*	1	0	1	1	0	U/L*	X	RCCR
B/W*	1	0	1	1	1	U/L*	X	TCOR
B/W*	1	1	0	0	0	U/L*	X	TDR
B/W*	1	1	0	0	1	U/L*	X	TMR
B/W*	1	1	0	1	0	U/L*	X	TCSR
B/W*	1	1	0	1	1	U/L*	X	TICR
B/W*	1	1	1	0	0	U/L*	X	TSR
B/W*	1	1	1	0	1	U/L*	X	TCLR
B/W*	1	1	1	1	0	U/L*	X	TCCR
B/W*	1	1	1	1	1	U/L*	X	TC1R

Table 2-2. Multiplexed Bus Addressing with Shift Right Selected

AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	Register
X	B/W*	0	0	0	0	0	U/L*	CCAR
X	B/W*	0	0	0	0	1	U/L*	CMR
X	B/W*	0	0	0	1	0	U/L*	CCSR
X	B/W*	0	0	0	1	1	U/L*	CCR
X	B/W*	0	0	1	0	0	U/L*	Reserved
X	B/W*	0	0	1	0	1	U/L*	Reserved
X	B/W*	0	0	1	1	0	U/L*	TMDR
X	B/W*	0	0	1	1	1	U/L*	TMCR
X	B/W*	0	1	0	0	0	U/L*	CMCR
X	B/W*	0	1	0	0	1	U/L*	HCR
X	B/W*	0	1	0	1	0	U/L*	IVR
X	B/W*	0	1	0	1	1	U/L*	IOCR
X	B/W*	0	1	1	0	0	U/L*	ICR
X	B/W*	0	1	1	0	1	U/L*	DCCR
X	B/W*	0	1	1	1	0	U/L*	MISR
X	B/W*	0	1	1	1	1	U/L*	SICR
X	B/W*	1	0	0	0	0	U/L*	RDR
X	B/W*	1	0	0	0	1	U/L*	RMR
X	B/W*	1	0	0	1	0	U/L*	RCSR
X	B/W*	1	0	0	1	1	U/L*	RICR
X	B/W*	1	0	1	0	0	U/L*	RSR
X	B/W*	1	0	1	0	1	U/L*	RCLR
X	B/W*	1	0	1	1	0	U/L*	RCCR
X	B/W*	1	0	1	1	1	U/L*	TC0R
X	B/W*	1	1	0	0	0	U/L*	TDR
X	B/W*	1	1	0	0	1	U/L*	TMR
X	B/W*	1	1	0	1	0	U/L*	TCSR
X	B/W*	1	1	0	1	1	U/L*	TICR
X	B/W*	1	1	1	0	0	U/L*	TSR
X	B/W*	1	1	1	0	1	U/L*	TCLR
X	B/W*	1	1	1	1	0	U/L*	TCCR
X	B/W*	1	1	1	1	1	U/L*	TC1R

Table 2-3. Separate Address Bus Addressing

AD14	AD13	AD12	AD11	AD10	AD9	AD8	Register
B/W*	0	0	0	0	0	U/L*	CCAR
B/W*	0	0	0	0	1	U/L*	CMR
B/W*	0	0	0	1	0	U/L*	CCSR
B/W*	0	0	0	1	1	U/L*	CCR
B/W*	0	0	1	0	0	U/L*	Reserved
B/W*	0	0	1	0	1	U/L*	Reserved
B/W*	0	0	1	1	0	U/L*	TMDR
B/W*	0	0	1	1	1	U/L*	TMCR
B/W*	0	1	0	0	0	U/L*	CMCR
B/W*	0	1	0	0	1	U/L*	HCR
B/W*	0	1	0	1	0	U/L*	IVR
B/W*	0	1	0	1	1	U/L*	IOCR
B/W*	0	1	1	0	0	U/L*	ICR
B/W*	0	1	1	0	1	U/L*	DCCR
B/W*	0	1	1	1	0	U/L*	MISR
B/W*	0	1	1	1	1	U/L*	SICR
B/W*	1	0	0	0	0	U/L*	RDR
B/W*	1	0	0	0	1	U/L*	RMR
B/W*	1	0	0	1	0	U/L*	RCSR
B/W*	1	0	0	1	1	U/L*	RICR
B/W*	1	0	1	0	0	U/L*	RSR
B/W*	1	0	1	0	1	U/L*	RCLR
B/W*	1	0	1	1	0	U/L*	RCCR
B/W*	1	0	1	1	1	U/L*	TC0R
B/W*	1	1	0	0	0	U/L*	TDR
B/W*	1	1	0	0	1	U/L*	TMR
B/W*	1	1	0	1	0	U/L*	TCSR
B/W*	1	1	0	1	1	U/L*	TICR
B/W*	1	1	1	0	0	U/L*	TSR
B/W*	1	1	1	0	1	U/L*	TCLR
B/W*	1	1	1	1	0	U/L*	TCCR
B/W*	1	1	1	1	1	U/L*	TC1R

Table 2-4. Indirect Addressing

B/W*	A4	A3	A2	A1	A0	U/L*	Register
B/W*	0	0	0	0	0	U/L*	CCAR
B/W*	0	0	0	0	1	U/L*	CMR
B/W*	0	0	0	1	0	U/L*	CCSR
B/W*	0	0	0	1	1	U/L*	CCR
B/W*	0	0	1	0	0	U/L*	Reserved
B/W*	0	0	1	0	1	U/L*	Reserved
B/W*	0	0	1	1	0	U/L*	TMDR
B/W*	0	0	1	1	1	U/L*	TMCR
B/W*	0	1	0	0	0	U/L*	CMCR
B/W*	0	1	0	0	1	U/L*	HCR
B/W*	0	1	0	1	0	U/L*	IVR
B/W*	0	1	0	1	1	U/L*	IOCR
B/W*	0	1	1	0	0	U/L*	ICR
B/W*	0	1	1	0	1	U/L*	DCCR
B/W*	0	1	1	1	0	U/L*	MISR
B/W*	0	1	1	1	1	U/L*	SICR
B/W*	1	0	0	0	0	U/L*	RDR
B/W*	1	0	0	0	1	U/L*	RMR
B/W*	1	0	0	1	0	U/L*	RCSR
B/W*	1	0	0	1	1	U/L*	RICR
B/W*	1	0	1	0	0	U/L*	RSR
B/W*	1	0	1	0	1	U/L*	RCLR
B/W*	1	0	1	1	0	U/L*	RCCR
B/W*	1	0	1	1	1	U/L*	TC0R
B/W*	1	1	0	0	0	U/L*	TDR
B/W*	1	1	0	0	1	U/L*	TMR
B/W*	1	1	0	1	0	U/L*	TCSR
B/W*	1	1	0	1	1	U/L*	TICR
B/W*	1	1	1	0	0	U/L*	TSR
B/W*	1	1	1	0	1	U/L*	TCLR
B/W*	1	1	1	1	0	U/L*	TCCR
B/W*	1	1	1	1	1	U/L*	TC1R

Table 2-5. Register Reset Values

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	Register	Note
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CCAR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CMR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	*	*	CCSR	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CCR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Reserved	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Reserved	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TMDR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TMCR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CMCR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	HCR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IVR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	IOCR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	ICR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	DCCR	
*	0	*	0	*	0	*	0	*	0	*	0	0	0	0	0	MISR	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	SICR	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	RDR	2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RMR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RCSR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RICR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RSR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RCLR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	RCCR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TCOR	
-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	TDR	2
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TMR	
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	TCSR	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TICR	3
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TSR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TCLR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TCCR	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	TC1R	

Note 1: The * indicates that the state of that bit is a function of the level present on the respective device pin.

Note 2: Both the receive and transmit FIFOs are emptied by reset.

Note 3: The two bits set to one in these registers are a result of the transmit FIFO being completely empty.



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3.1 FUNCTIONAL DESCRIPTION

Chapter 3 explains and illustrates the various functional capabilities of the USC including receive, transmit, interrupt, DMA, etc.

3.2 RECEIVER

The receiver performs all the functions necessary to convert serial data back to parallel for the processor.

Serial data on the RxD pin is sampled on the rising edge of the /RxC (receive clock) pin for all formats and encoding modes, except for Biphase encoding mode where both /RxC edges are used for data sampling. The serial data is received with the least significant bit first. The data, however, can be stored in LSB or MSB first format in the output FIFO's (LSB after reset). It is controlled by the CCAR D15-11. In addition, the receiver can read the serial data as words and put the byte first received in bits 15-8 of the word and the byte which followed to occupy bits 7-0 of the same word (default setting after reset). Such order can be swapped and both arrangements are controlled by the CCAR D15-11.

The receive data FIFO is 32 bytes deep and data can be read either as bytes or words. The /DCD pin is a general purpose I/O pin for the receiver. When the receiver is enabled with auto enables (RMR), this pin should be programmed as an input. The sync pin is multiplexed with the DCD pin and its activity is described in IOCR D13-12. The sync signal can also be programmed as an output through the /RxC pin (IOCR 2-0).

Rx character length is 1- to 8-bits per character. The character length may not be changed on the fly as the internal data paths are character-length dependent. Character length may, however, be changed between characters in the asynchronous mode while the receiver is in hunt mode in all synchronous modes.

Other features of the receiver include:

Parity: Even, odd, space, or mark (RMR D7-5)

CRC: CRC-CCITT, CRC-16, CRC-32 (RMR D12-9)

CHAPTER 3

DETAILED FUNCTIONAL DESCRIPTION

Data Decoding: NRZ, NRZB, NRZI-Mark, NRZI-Space, Biphase-Mark, Biphase-Space, Biphase-Level and Differential Biphase-Level (RMR D15-13).

3.3 TRANSMITTER

The transmitter performs all the necessary functions to convert parallel data from the processor into the appropriate serial bit stream.

Serial data on the TxD pin is sent on the falling edge of the /TxC (transmit clock) pin for all formats and encoding modes except for Biphase encoding mode where both /TxC edges are used for data transmission. The serial data is transmitted with the least significant bit first. The data, however, can be stored in LSB or MSB first format in the input FIFO's (LSB after reset). It is controlled by the CCAR D15-11. In addition, the transmitter can be programmed to shift bits 15-8 of a word first (after reset), followed by bit 7-0 of the same word, or vice versa being controlled by the CCAR D15-11.

The transmit data FIFO is 32 bytes deep and data can be written to the USC in byte or word. The /CTS pin is a general purpose I/O pin for the transmitter. When the transmitter is enabled with autoenables (TMR D1-0), this pin should be programmed as an input. The /RTS signal can be implemented through the /TxREQ pin (IOCR D11-10).

The transmit character length can be 1-8 bits long and the length can be changed at any time. The new character length takes effect on the next character loaded into the transmit shift register. One is automatically added to the programmed character length in asynchronous modes if parity is enabled. The data bits must always be right-justified in the TDR (Transmit Data Register).

Other features of the transmitter: Parity, CRC and Data Encoding are the same as described in the receiver section (3.1), except for programming which is in the TMR. Send break can be implemented by programming the IOCR D7-6 to send "0" on the TxD pin.

3.4 BAUD RATE GENERATORS (BRG)

Each channel in the USC contains two baud rate generators. Each generator consists of a 16-bit time constant register and a 16-bit down counter. In operation, the counter decrements with each BRG clock, with the time constant automatically reloaded when the count reaches zero. The output of the BRG toggles when the counter reaches a count of one-half of the time constant and again when the counter reaches zero. A new time constant may be written at any time but the new value will not take effect until the next load of the counter. The outputs of both BRGs are sent to the clock multiplexer for use internally or externally. The BRG output frequency is related to the BRG input clock frequency by the following formula:

$$\text{Output frequency} = \frac{\text{Input frequency}}{(\text{time constant} + 1)}$$

This allows an output frequency in the range of 1 to 1/65536 of the input frequency, inclusive. The output of the BRG is always a square wave.

Each channel contains two 5-bit counters, which may be programmed to divide an input clock by 4, 8, 16 or 32. The inputs of these two counters are sent to the clock multiplexer. The counters may be used as prescalers for the baud rate generators, or to provide a stable transmit clock from a common source when the DPLL is providing the receive clock.

The counter in the BRG automatically reloads the time constant when a count of zero is reached in continuous mode and stops at the count of zero when operating in the single-cycle mode.

CCAR C15-1 contains instructions to load TC0 and/or TC1 to BRG0 and/or BRG1 respectively. In single-cycle mode (HCR D5-1), it will also start the counting operation in BRG0 and/or BRG1.

Both BRGs clock source can be programmed from CTR0 output, counter 1 (CTR1) output, /RxC pin or /TxC pin (CMCR).

The counters (CTR's) clock sources are:

/RxC pin or /TxC pin (CMCR)

The BRGs output is controlled by (CMCR, IOCR):

Transmit Clock Source (CMCR D5-3)

Receive Clock Source (CMCR D2-0)

/TxC pin (IOCR D5-3)

/RxC pin (IOCR D2-0)

The time constant registers (TC0R, TC1R) hold the time constant used by the baud rate generator BRG0, BRG1, respectively. The TC0R is a read/write register, but the value returned during a read depends on the state of the TC0R read Count/TC control bit in the RICR. Similarly, the TC1R is controlled by the corresponding bit in the TICR. If the TC0R (TC1R) Read Count/TC control bit in the RICR (TICR) is set to zero, the time constant is returned during the read; otherwise the current count in the counter is returned.

The HCR (D4,0) are used to enable and disable the BRG. A "0" in this bit disables the BRG, without disturbing the current count in the counter.

A "1" in this bit enables the BRG to continue counting from the current count in the counter. The load TC0/TC1 command in the CCAR is used to load the time constant into the counter.

3.5 DIGITAL PHASE-LOCKED LOOP (DPLL)

Each channel in the USC contains a Digital Phase-Locked Loop (DPLL) to recover clock information from a data stream with NRZI or Biphase encoding. The DPLL is driven by a clock that is nominally 8, 16 or 32 times the receive data rate. The DPLL uses this clock, along the data stream, to construct a clock for the data. This clock may then be routed to the receiver, transmitter or both, or to a pin for external use. In all modes the DPLL counts the input clock to create nominal bit times. As the clock is counted, the DPLL watches the incoming data stream for transitions. Whenever a transition is detected, the DPLL makes a count adjustment (during the next counting cycle), to produce an output clock which tracks the incoming bit cells. The DPLL provides properly phased transmit and receive clocks to the clock multiplexer.

The DPLL clock rate is programmed in HCR D11-10. Note that the clock rate is independent of the data encoding mode used. Clock rate can be 32x, 16x or 8x of the data rate.

D9-8 of the CCSR control which edges (rising and/or falling) are used by the DPLL to achieve and maintain synchronization.

Other bits in the CCSR (D12-10) report the status of missing transitions in the bit cells. They also report successive missing transitions and a loss of synchronization. Bits are latched until cleared by software.

The DPLL is automatically enabled when the DPLL mode is selected from D9-8 of HCR. Possible selections of DPLL mode are NRZ/NRZI, biphase-mark/space and biphase-level.

In NRZ/NRZI mode (Figure 3-1), the DPLL Rx output and the DPLL Tx output are identical and such outputs can become the /RxC pin and /TxC pin outputs, respectively (IOCR D2-0, D5-3).

The following diagram shows the timing of the DPLL Rx/Tx output:

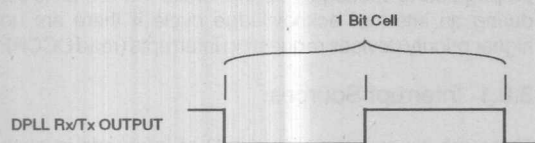


Figure 3-1. NRZ/NRZI Modes

In biphase mark (FM1), biphase space (FM0) and biphase-level (Manchester), the DPLL Tx output timing is the same as in NRZ/NRZI mode. However, the DPLL Rx output is different (Figure 3-2).

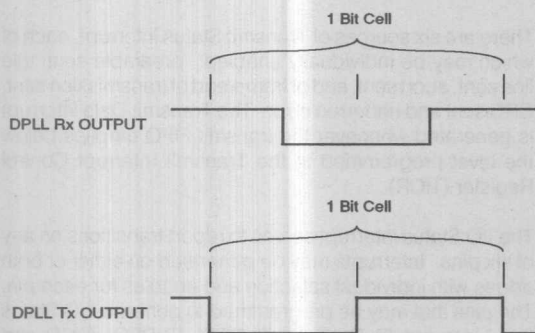


Figure 3-2. Any Biphase Mode

3.6 CHARACTER COUNTERS

The character counters are used in synchronous message oriented protocols, e.g., SDLC and Bisync. Each channel in the USC contains a 16-bit character counter for both receiver and transmitter. The receive character counter may be preset, either under software control (CCAR D15-

11; Reload Receive Character Count Command) or automatically at the beginning of a receive message (CCAR D15-11: Receive DMA Trigger Command).

The Receive Count Limit Register (RCLR) holds the starting count value for the receive character counter.

Receive character counting operation is disabled while this register contains all zeros. A non-zero value in this register indicates the maximum allowable number of bytes of data to be received in this frame or message. The number in this register is the number of data bytes only; it does not include the number of bytes in the receive status block, if any.

Any receive character counting operation in progress is unaffected by writing a new value to this register, even if the new value is zero, which disables the character counting operation.

Writing a non-zero value to this register does not, in itself, enable the receive character counting operation. Rather, the character counting operation is enabled/disabled and the receive character counter is loaded by the trigger receive DMA command, the reload receive character count command, the receive FIFO purge command or receipt of an opening flag of sync character (CCAR).

Writing this register with all ones allows the length of the frame or message to be easily determined; it is just the ones complement of the value in the (Receive Character Count Register) RCCR or the (Receive Character Count Holding Register) RCHR.

The counter decrements with each receive character transferred to the FIFO, and at the end of the receive message the current value in the counter is automatically loaded into a 4-deep (Receive Character Count) RCC FIFO. The current count value can now be read in the (Receive Character Count Register) RCCR. The second word of the Receive Status Block Register (RSBR), if used (CCR), is the current value in the Receive Character Count Holding Register (RCHR).

The RCC FIFO can be cleared through programming D13 of CCSR. Two status bits from the RCC FIFO, Valid and Overflow, can be read from D14 and 13 from CCSR.

The RCCR FIFO allows DMA transfer of data to proceed without CPU intervention at the end of a received message, as the values in the FIFO allow the CPU to determine message boundaries in memory. Similarly, the transmit character counter may be loaded either under software control or automatically at the beginning of a transmit message. The counter is decremented with each write to the transmit FIFO. When the counter has decremented to

zero, and that byte is sent, the transmitter automatically terminates the message in the appropriate fashion (usually CRC and the closing flag or sync character) without requiring CPU intervention.

3.7 POLLING

Polling avoids interrupts and is the simplest mode to implement. In this mode, the software must poll the USC to determine when data is to be written or read to or from the USC. All interrupts have to be disabled (ICRD15). The registers in the USC are automatically updated to reflect current status. The CPU polls the Daisy-Chain Control Register (DCCR) to determine status changes and then reads the appropriate status register to find and respond to the change in status. USC status bits are grouped according to function to simplify this software action.

3.8 INTERRUPT

The Master Interrupt Enable (MIE) bit in the ICR D15 globally enables or disables interrupts within a channel.

When the USC responds to an interrupt acknowledge from the CPU, an interrupt vector may be placed on the data bus. This vector is held in the Interrupt Vector Register (IVR). To speed interrupt response time, the USC can modify three bits in this vector to indicate which type of interrupt is being requested (IVR). These three bits are maskable by the Vector and Includes Status Level Control Field (ICR).

Each of the six sources of interrupts in each channel in the USC (Receive Status, Receive Data, Transmit Status, Transmit Data, I/O Status and Device Status) has three bits associated with the interrupt source: Interrupt Pending (IP), Interrupt Under Service (IUS) and Interrupt Enable (IE). If the IE bit for a given source is set, then that source can request interrupts. Note that individual sources within the six groups also have interrupt enable bits which must be set (ICR D7-0). Even though the IE bits can be reset, it will not affect the IP bit being set by the interrupt condition.

The other two bits are related to the interrupt priority chain. A channel in the USC may request an interrupt only when no higher priority interrupt source is requesting one, e.g.,

when IEI is High for the channel. In this case, the channel activates the /INT signal. The CPU then responds with an interrupt acknowledge cycle, and the interrupting channel places a vector on the data bus.

In the USC, the IUS bit signals that an interrupt request is being serviced. If an IUS is set, all interrupt sources of lower priority within the channel and external to the channel are prevented from requesting interrupts. The internal interrupt sources are inhibited by the state of the internal daisy-chain, while lower priority devices are inhibited by the IEO output of the channel being pulled Low and propagated to subsequent peripherals. An IUS bit is set during an interrupt acknowledge cycle if there are no higher priority devices requesting interrupts (read DCCR).

3.8.1 Interrupt Sources

There are six sources (Table 3-1) of interrupts in each channel: Receive Status, Receive Data, Transmit Data, I/O Status and Device Status, prioritized in that order within the channel. There are six sources of receive Status interrupt, each of which may be individually enabled: receiver exited hunt, received idle line, received break/abort, received code violation/end of transmission/end of frame, parity error and overrun error. The Receive Data interrupt is generated whenever the receive FIFO fills with data beyond the level programmed in the Receive Interrupt Control Register (RICR).

There are six sources of Transmit Status interrupt, each of which may be individually enabled: preamble sent, idle line sent, abort sent, end of frame/end of transmission sent, CRC sent and underrun error. The Transmit Data interrupt is generated whenever the transmit FIFO empties below the level programmed in the Transmit Interrupt Control Register (TICR).

The I/O Status interrupt serves to report transitions on any of six pins. Interrupts may be generated on either or both edges with individual selection and enables for each pin. The pins that may be programmed to generate I/O Status interrupts are /RxC, /TxC, /RxREQ, /TxREQ, /DCD and /CTS. These interrupts are independent of the programmed function of the pins. The Device Status interrupt has four individually enabled sources: receive character count FIFO overflow, DPLL sync acquired, BRG1 zero count and BRG0 zero count.

Table 3-1. USC Interrupt Conditions/Sources

Registers Involved	Interrupt Conditions	Sources
		Highest Priority
RICR/ RCSR	Rx exited hunt	
	Rx idle line	
	Rx break/abort	
	Rx code violation/ EOT/EOF	
	Parity error	Receive Status
	Overrun error	
		Receive Data
TICR/ TCSR	Preamble sent	
	Idle line sent	
	Abort sent	
	EOF/EOT sent	
	CRC sent	Transmit Status
	Underrun error	
		Transmit Data
SICR/ MISR	RxC	
	TxC	
	RxREQ	
	TxREQ	
	DCD	I/O Status
	CTS	
	RCC FIFO Overflow	
	DPLL Sync Required	
	BRG1 zero count	Device Status
	BRG0 zero count	
		Lowest Priority

an interrupt request will be generated. A value "n" in this byte indicates that "n+1" bytes must be present in the FIFO before the interrupt request will be generated.

3.8.1.3 Transmit status interrupt: The Transmit Interrupt Control Register (TICR) contains control bits for the transmitter. The upper byte controls the interrupt and DMA request levels of the FIFO and reports the current fill level of the FIFO, while the lower byte contains the Interrupt Enable IE bits for the sources of transmit status interrupts. The Transmit Command/Status Register (TCSR) contains commands and status for the transmitter and works in conjunction with the programming of the TICR.

3.8.1.4 Transmit data interrupt: After the "Select FIFO Interrupt Level" command in the TCSR, the "Transmit FIFO Control and Status Field" in the TICR controls the number of bytes which must be present in the transmit FIFO before an interrupt request will be generated. A value "n" in this byte indicates that "n+1" byte locations must be available in the FIFO before the interrupt request will be generated.

3.8.2 I/O Status and Device Status Interrupts

The Status Interrupt Control Register (SICR) contains the control bits and fields for the various sources of I/O status and device status interrupts, while the Miscellaneous Interrupt Status Register (MISR) contains the command and status bits for the same interrupts. Therefore, the RICR/RCSR, TICR/TCSR and SICR/MISR, work in pairs (Figure 3-3).

3.8.1.1 Receive status interrupt: The Receive Interrupt Control Register (RICR) contains control bits for the receiver. The upper byte controls the interrupt and DMA request levels of the FIFO and reports the current fill level of the FIFO, while the lower byte contains the Interrupt Enable IE bits for the sources of receive status interrupts. The Receive Command/Status Register (RCSR) contains commands and status for the receiver and works in conjunction with the programming of the RICR.

3.8.1.2 Receive data interrupt: After the "Select FIFO Interrupt Level" command in the RCSR, the "Receive FIFO Control and Status Field" in the RICR controls the number of bytes which must be present in the receive FIFO before

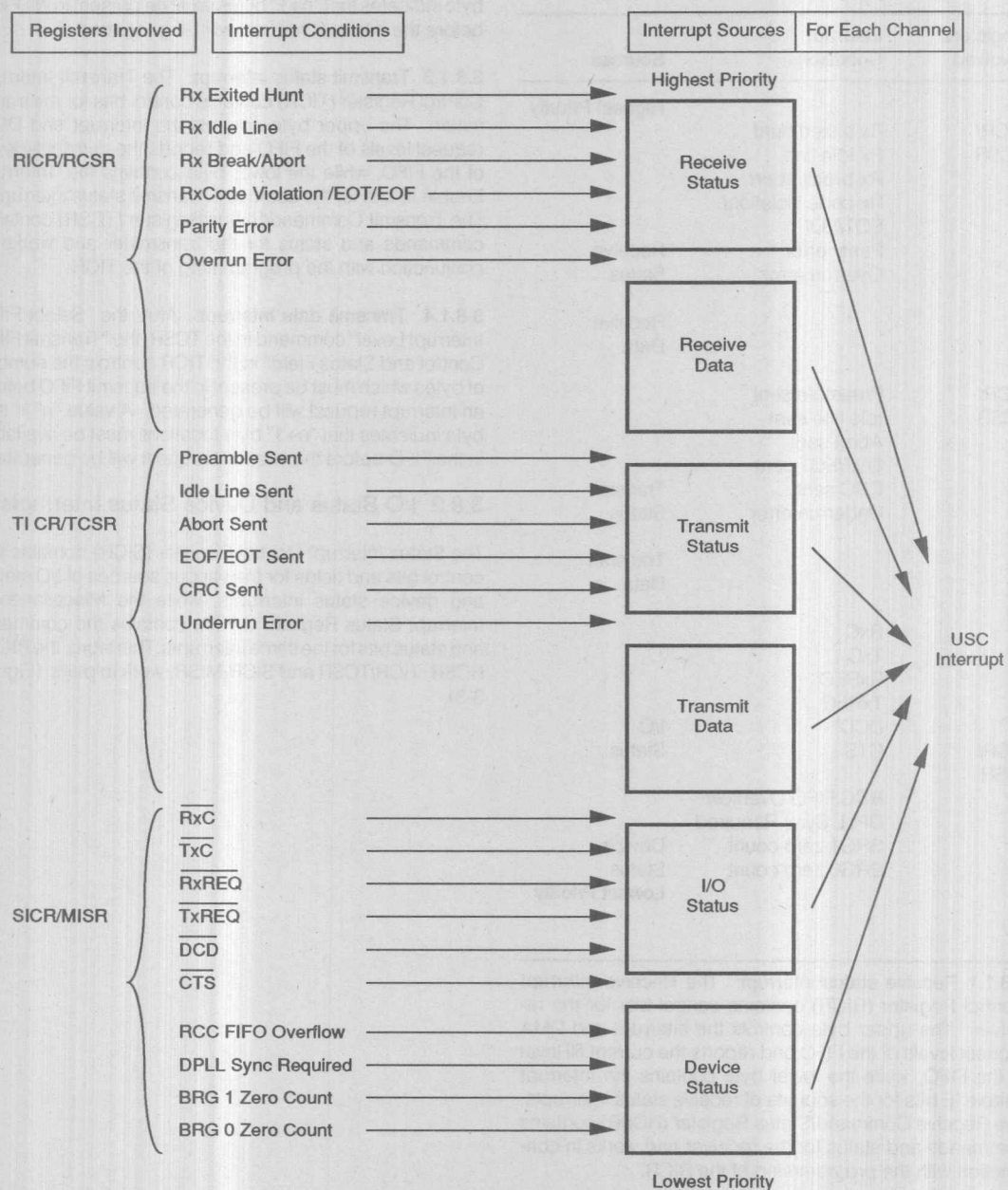


Figure 3-3. USC Interrupt Sources

More than one interrupt condition can be latched and generate an interrupt at one time within an interrupt source such as I/O status. The programmer should decide which interrupt condition should be serviced first.

Both Channel A and Channel B have their own IEI and IEO pins. This means that both channels can operate independently and the user can configure the interrupt priority of either channel using the IEI and IEO pins.

3.8.3 Interrupt Without Acknowledge

When the /INT line goes low, an interrupt request is occurring. The processor can respond by resetting the corresponding IP or IE bit of the interrupting condition. Note that the /SITACK and the /PITACK have to be tied high. The interrupting condition can be determined by reading the status register in the DCCR.

3.8.4 Interrupt With Acknowledge With Vector

The /SITACK (Status Interrupt Acknowledge) is a status input signal to the USC. During an interrupt acknowledge cycle, this signal is either sampled by /AS, /DS, or the /RD signals indicating that an interrupt acknowledge cycle is in progress. The rising edge of /DS or /RD will be used to sample the valid vector.

The last interrupt control signal is the /IVACK (Interrupt Vector Acknowledge).

The Interrupt Vector Wait Control Bit in the BCR (D1) is used to select the type of acknowledge signal present on the /IVACK pin during an interrupt acknowledge cycle.

The CPU must not terminate the interrupt acknowledge cycle until the device has released this signal, indicating that the internal daisy chain has settled.

0 in the Interrupt Wait Control Bit enables the /IVACK output to function as a Ready signal, going Low during an interrupt acknowledge cycle when the internal daisy-chain has settled and the vector is available on the data bus.

1 in the Interrupt Wait Control Bit enables the /IVACK output to function as a Wait signal, going Low at the beginning of an interrupt acknowledge cycle and remaining Low until the internal daisy-chain has settled and the vector is available on the data bus.

/SITACK and/or /PITACK should be tied high if not needed.

3.8.5 Interrupts (With Acknowledge Without Vector)

The same timing activities as described above occur for interrupts, except that there is no valid vector during the interrupt acknowledge cycle. ICR D13 controls vector/no vector interrupt.

3.9 DMA

The USC accommodates block transfers via DMA through the /RxREQ, /TxREQ, /RxACK and /TxACK pins. The /RxREQ signal is activated when the fill level of the receive FIFO exceeds the value programmed in the RICR. The DMA may respond with either a normal bus transaction or by activating the /RxACK pin to read the data directly (fly-by transfer). The /TxREQ signal is activated when the empty level of the transmit FIFO falls below the value programmed in the TICR. The DMA may respond either with a normal bus transaction or by activating the /TxACK pin to write the data directly (fly-by transfer). The /RxACK and /TxACK pin functions for this mode are controlled by the Hardware Configuration Register (HRC). Then, using the /RxACK and /TxACK pins to transfer data, no chip select is necessary; these are dedicated strobes for the appropriate FIFO.

The Receive DMA Trigger Command (CCAR D15-11) enables the receive DMA request, which is disabled at the end of a frame or message only if the "wait for RxDMA trigger" control bit in the CCR is set to one. The same mechanism applies to the Transmit DMA.

To initiate a DMA request, select the FIFO request level in the RICR and TICR and program the IOCR to select the /RxREQ and /TxREQ as request outputs.

3.9.1 Channel Load DMA

The Channel Load DMA Trigger command in the CCAR triggers the transmit DMA request to load the registers in the channel and overrides the function programmed for the /TxREQ pin in the IOCR for the duration of the channel load operation. It is not necessary to fill in the FIFO level in RICR and program the IOCR to select the /RxREQ or /TxREQ as request outputs.

During a channel load, the DMA transfers addresses and data to the CCAR. The address pointer functions normally in this mode and either byte or word accesses may be used. If ordinary write cycles are used to write data to the device, the data must be written through the CCAR using the address pointer. If the /TxACK signal is used for fly-by transfers to the channel, the destination is the CCAR or the register pointed to by the address pointer in the CCAR.

The channel load operation is terminated when the DMA Continue bit in the CCAR is cleared. Upon termination of the channel load operation, the /TxREQ pin will resume the function selected in the IOCR. Bit 7 in the CCAR is used to control the length of the channel load DMA transfer.

This bit is used only during a channel load DMA transfer and must be set to 1 during the first channel load DMA transfer. This bit is ignored except during the channel load operation. The address pointer written to the CCAR with this bit selects the ultimate destination for the data.

If bit 7 in the CCAR is set to 1 with the address written during the channel load, the channel load operation continues. In this case, if the address written to the CCAR is neither the word address of the CCAR nor the address of the lower byte of the CCAR, another address-data pair will be requested by the channel after the data for this address has been transferred. If the address written to the CCAR is the word address of the CCAR or the address of the lower byte of the CCAR, no data accompanies the address and the next transfer is another address to the CCAR.

If bit 7 in the CCAR is set to 0 with the address written during the channel load, the channel operation is terminated and the /TxREQ pin is released to its normal function. In this case, if the address written is the word address of the

CCAR or the address of the lower byte of the CCAR, no further transfers are requested and the pointer is not cleared, if pointing to the lower byte of the CCAR. If the address written is neither the word address of the CCAR, nor the address of the lower byte of the CCAR, another transfer is requested to transfer the data to the addressed register and then the channel load operation is terminated.

3.10 CLOCK OPTIONS

No system clock is required for the USC.

The clock multiplexer (IOCR) in each channel selects the clock source for the various blocks in the channel, as well as selecting an internal clock signal to potentially be sent to either the /RxC or /TxC pin.

3.11 DATA ENCODING/DECODING

The USC may be programmed to encode and decode the serial data in any of seven different ways as shown in Figure 3-4. The transmitter encoding method is selected (TMR) independently of the receiver decoding method (RMR). The DPLL is used to decode the receiving data.

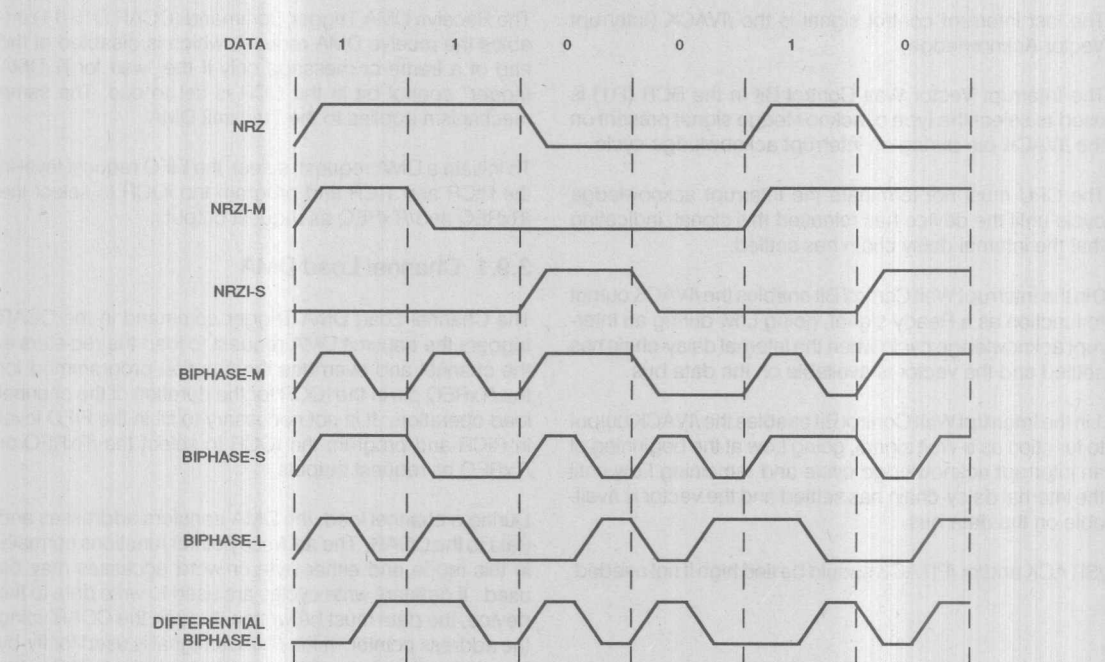


Figure 3-4. Data Encoding

3.11.1 NRZ

In NRZ, a 1 is represented by a high level for the duration of the bit cell and a 0 is represented by a Low level for the duration of the bit cell.

3.11.2 NRZI-MARK

In NRZI-Mark, a 1 is represented by a transition at the beginning of bit cell. That is, the level present in the preceding bit cell is reversed. A 0 is represented by the absence of a transition in the bit cell.

3.11.3 NRZI-SPACE

In NRZI-Space, a 1 is represented by the absence of a transition in the bit cell. That is, the level present in the preceding bit cell is maintained. A 0 is represented by a transition at the beginning of the bit cell.

3.11.4 BIPHASE-MARK

In Biphase-Mark, a 1 is represented by a transition at the beginning of the bit cell and another transition at the center of the bit cell. A 0 is represented by a transition at the beginning of the bit cell only.

3.11.5 BIPHASE-SPACE

In Biphase-Space, a 1 is represented by a transition at the beginning of the bit cell only. A 0 is represented by a transition at the beginning of the bit cell and another transition at the center of the bit cell.

3.11.6 BIPHASE-LEVEL

In Biphase-Level, a 1 is represented by a High during the first half of the bit cell and a Low during the second half of the bit cell. A 0 is represented by a Low during the first half of the bit cell and a High during the second half of the bit cell.

3.11.7 DIFFERENTIAL BIPHASE-LEVEL

In Differential Biphase-Level, a 1 is represented by a transition at the center of the bit cell, with the opposite polarity from the transition at the center of the preceding bit cell. A 0 is represented by a transition at the center of the bit cell with the same polarity as the transition at the center of the preceding bit cell. In both cases there may be transitions at the beginning of the bit cell to set up the level required to make the correct center transition.

3.1.1.1.1.1

in the case of a transition from a state to another state, the transition is labeled with the name of the transition function. The transition function is a function from the set of states to the set of states.

3.1.1.1.1.2

in the case of a transition from a state to another state, the transition is labeled with the name of the transition function. The transition function is a function from the set of states to the set of states.

3.1.1.1.1.3

in the case of a transition from a state to another state, the transition is labeled with the name of the transition function. The transition function is a function from the set of states to the set of states.

3.1.1.1.1.4

in the case of a transition from a state to another state, the transition is labeled with the name of the transition function. The transition function is a function from the set of states to the set of states.

3.1.1.1.2.1

in the case of a transition from a state to another state, the transition is labeled with the name of the transition function. The transition function is a function from the set of states to the set of states.

3.1.1.1.2.2

in the case of a transition from a state to another state, the transition is labeled with the name of the transition function. The transition function is a function from the set of states to the set of states.

3.1.1.1.2.3

in the case of a transition from a state to another state, the transition is labeled with the name of the transition function. The transition function is a function from the set of states to the set of states.

CHAPTER 4

MODES OF OPERATION

AUGUST 1989

4.1 INTRODUCTION

The USC provides two independent full-duplex channels which are user programmable for use in any asynchronous or synchronous protocol. This includes:

- Asynchronous protocol
 - asynchronous
 - isochronous
 - asynchronous with code violation
 - NBIP
- Byte-oriented protocol
 - external sync
 - mono sync
 - bisync
 - transparent bisync
 - IEEE 802.3

- Bit-oriented protocol
 - SDLC/HDLC

4.2 ASYNCHRONOUS

In this protocol, data is transmitted at irregular intervals. Each data is framed with start, stop and option parity bit before transmission. The transmission of data begins when the line makes a transition from mark to space condition. This transition allows the receiver to determine the cell boundaries and sample each bit in the center of the bit cell. Figure 4-1 shows a typical USC asynchronous data format.

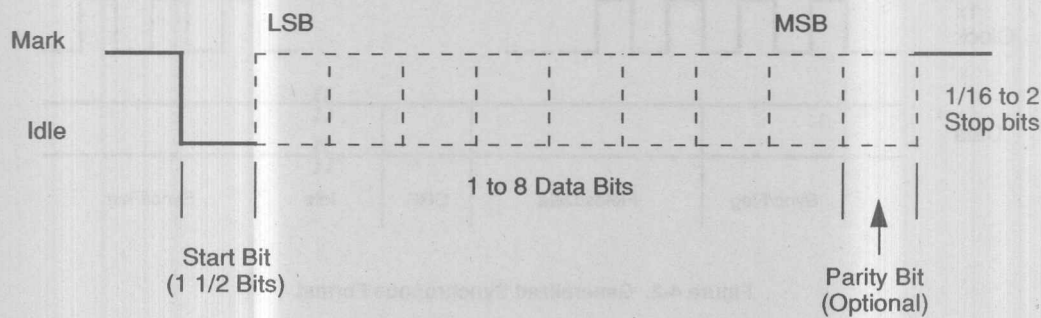


Figure 4-1. USC Async Data Format

As shown in Figure 4-1, async formatted data has the following fields:

- Start Bit - Indicates the beginning of data; a mark to space transition where the space condition lasted at least one-half of a bit time.
- Data Field - One to eight bits long.
- Optional Parity Bit - Used for checking character validity. The USC supports four types of parity bits:
 - Even - Even number of ones in data and parity bit
 - Odd - Odd number of ones in data and parity bit
 - Space - Parity bit is always space (zero)
 - Mark - Parity bit is always mark (one)
- Stop Bit(s) - Provides a minimum interval between two data bytes transmitted back-to-back. This interval lasts 1/16 to 2 bit times in programmable 1/16 bit steps.

There are three special conditions in asynchronous communications:

- Framing Error - A non-zero data and a space stop bit. This is an indication of bit misalignment within one or more data bytes.
- Break - A zero data and a space stop bit. This condition may persist for an integral number of data byte times or for a fixed interval. The purpose is to get the receiver's attention.

- Parity Error - Discrepancy between parity computation on data and parity bit transmitted.

4.3 SYNCHRONOUS

This type of transmission requires that clock information be transmitted along with the data. The clock and data could be encoded or transmitted via a modem that encodes clock information in the modulation process. In any case, data is sent at a defined rate by the transmitter.

This clock information, after being retrieved by the DPLL, is used by the receiver to sample the incoming data. Normally, the optimum sample time corresponds with the middle of the bit cell. A transition in the middle of the bit cell tells the receiver whether the sampled bit value is a one or zero.

Synchronous transmitted data rates are much higher than asynchronous data rates. Also, synchronous data is sent without gaps between characters. The higher data rate and contiguous data requires buffering at both the transmitter and receiver ends.

Using the clock information, the receiver is able to sample the incoming data bits correctly. These sampled bits are grouped into characters. From these characters, the receiver can determine the exact fields in synchronous format (Figure 4-2). The synchronous format depends on the synchronous protocol used and may be either byte- or bit-oriented.

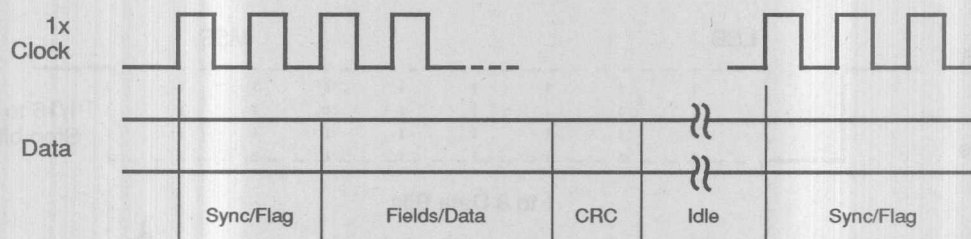


Figure 4-2. Generalized Synchronous Format

4.3.1 Byte-oriented Synchronous Protocol

In this protocol, data is transmitted in message blocks that are preceded by 8- or 16-bit predefined synchronous characters. Within the message blocks, special control characters, such as DLE, STX and ETX, delimit the control fields. Typically, byte-oriented synchronous protocol is

limited to half-duplex mode. Although data transmission is continuous, there are times where no data transmission takes place. In these instances synchronous characters may be transmitted to maintain receiver synchronization.

4.3.2 Bit-oriented Synchronous Protocol

Bit-oriented protocols may be used in half- or full-duplex modes and are less dependent on special control characters. Commonly used bit-oriented protocols are Synchronous Data Link (SDLC) and High-Level Data Link Control (HDLC).

Synchronous Data Link Control mode (SDLC) uses synchronization characters similar to Bisync and Monosync modes (such as flags and pad characters), but it is bit-oriented instead of byte-oriented protocol.

Any data communication link involves at least two stations. The station that is responsible for the data link and issues the commands to control the link is called the "primary

station." The other station is a "secondary station." Not all information transfers need to be initiated by the primary station. In SDLC mode, a secondary station can be the initiator.

The basic format for SDLC is a "frame" (Figure 4-3). The information field is not restricted in format or content and can be of any reasonable length (including zero). Its maximum length is that which can be expected to arrive at the receiver error-free most of the time. Hence, the determination of maximum length is a function of communication channel error rate.

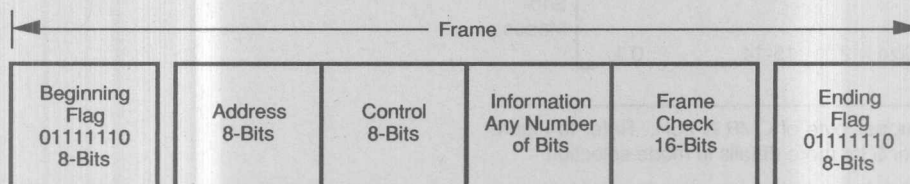


Figure 4-3. SDLC Message Format Frame

The two flags that delineate the SDLC frame serve as reference points when positioning the address and control fields, and they initiate the transmission error check. The ending flag indicates to the receiving station that the 16-bits just received constitute the frame check. The ending flag could be followed by another frame, another flag, or an idle. This means that when two frames follow one another, the intervening flag may simultaneously be the ending flag of the first frame and the beginning flag of the next frame. Since the SDLC mode does not use characters of defined length, but rather works on a bit-by-bit basis, the 01111110 (7EH) flag can be recognized at any time.

To ensure that the flag is not sent accidentally, SDLC procedures require a binary "0" to be inserted by the transmitter after the transmission of any five contiguous "1's." Inserted and removed "0's" are not included in the CRC calculation.

The address field is eight bits long and designates the number of the secondary station to which the commands or data from the primary station are sent. The control field is eight bits long and is used to initiate all SDLC activities (see Section 3.6).

The frame check sequence is typically 16-bits long and contains the generated CRC for that frame. CRC computation is based on all data transmitted between the opening and closing flags, excluding inserted zeros. The CRC generator for available binary polynomials is:

- CRC-16 $X^{16} + X^{15} + X^2 + 1$
- CRC-22 (Ethernet polynomial) $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^9 + X^7 + X^5 + X^4 + X^2 + 1$
- CRC-CCITT-1 $X^{16} + X^{12} + X^5 + 1$, preset to ones
- CRC-CCITT-0 $X^{16} + X^{12} + X^5 + 1$, preset to zeros

4.4 MODE SELECTION

Selecting the data communication mode in the USC involves only programming the Channel Mode Register (CMR). The lower byte (7-0) of CMR selects the receiver mode and the higher byte (15-8) selects the transmitter mode. Within these bytes, the upper four bits are used to program the receiver and transmitter sub-modes. For example, programming CMR for async mode in the transmitter is as follows:

Description	Bits in CMR	Bit Value
Async Mode	11-8	0000
Tx Clock Rate = 64x	13-12	10
Tx Stop Bit Size = 2	15-14	0 1

Tx
Sub-
Modes

Hence, the upper byte of CMR is 60H. Refer to Figure 5-3 in Chapter 5 for more details in mode selection.



AUGUST 1989

CHAPTER 5

REGISTER DESCRIPTIONS

5.1 INTRODUCTION

In general, initializing the USC involves setting up the pin configuration and functional units, enabling functional units, and setting up the interrupts. It is absolutely essential that all functional units are set up first, then enabled, and lastly, the interrupt conditions are set.

5.1.1 Pin Configurations

There are nine pins that can be configured; namely /RxC, /TxC, /TxD, /RxREQ, /TxREQ, /DCD, /CTS, /RxACK and /TxACK. The programmable features for these pins can be found in registers MISR, IOCR, SICR and HCR. The latch conditions for these pins are set in MISR, pin definitions in IOCR and interrupt control status through SICR. Only /RxACK and /TxACK are configured via HCR.

5.1.2 Setting Up Functional Units

Functional units in the USC are Receiver, Transmitter, BRG0, BRG1, DPLL, CTR0 and CTR1. The programmable features for these units can be found in registers CMR, CMCR, RMR, RCLR, CCR, TMR, TCLR, HCR, MISR, TCOR, TC1R and CCSR. Features for the receiver are found in registers CMCR, RMR, RCLR, and CMR; for the transmitter: registers CMCR, TMR, TCLR and CMR. The programmable features for the BRGs are found in HCR, CMCR, MISR, TCOR, and TC1R. Registers CMR, HCR, CCSR and MISR are used to program the DPLL. Lastly, the counters are programmed using CMCR and HCR.

5.1.2.1 Enabling Functional Units. The transmitter and receiver are enabled using registers TMR and RMR, respectively. Register HCR is used to enable the BRGs. The DPLL is enabled when the mode is selected via register HCR.

5.1.3 Setting Up the Interrupts

Registers involved in setting up the interrupts are ICR, MISR, IVR, DCCR, RICR, TICR and CCR. Sources of interrupts are programmed via register ICR and the interrupt vector is defined in IVR. The daisy-chain interrupts are prepared via DCCR. The transmit and receive interrupt conditions are enabled in TICR and RICR, respectively. DMA interrupts are programmed via register CCR. Finally, the master interrupt is enabled in register ICR.

A summary on programming the USC is shown in the following table (Table 5-1).

5.2 REGISTER DESCRIPTION

This section describes the function of the various bits in the registers of the device. Throughout this section the following conventions will be used:

Control bits may be written and read by the CPU and will not be modified by the device. Command bits may be written by the CPU to initiate an action in the device and will be read as zeros. Status bits are controlled by the device and may be read to check device status. Any writes to status bits are ignored by the device. Command/status bits are controlled by both the device and the CPU. They may be written and read by the CPU and may also be modified by the device.

Reserved bits are not used in this implementation of the device and may or may not be physically present in the device. Reserved bits that are physically present will be readable and writable but reserved bits that are not present will always be read as zero. To ensure compatibility with future versions of the device reserved bits should always be written with zeros. Reserved commands should not be used for the same reason.

Table 5-1. Programming the USC

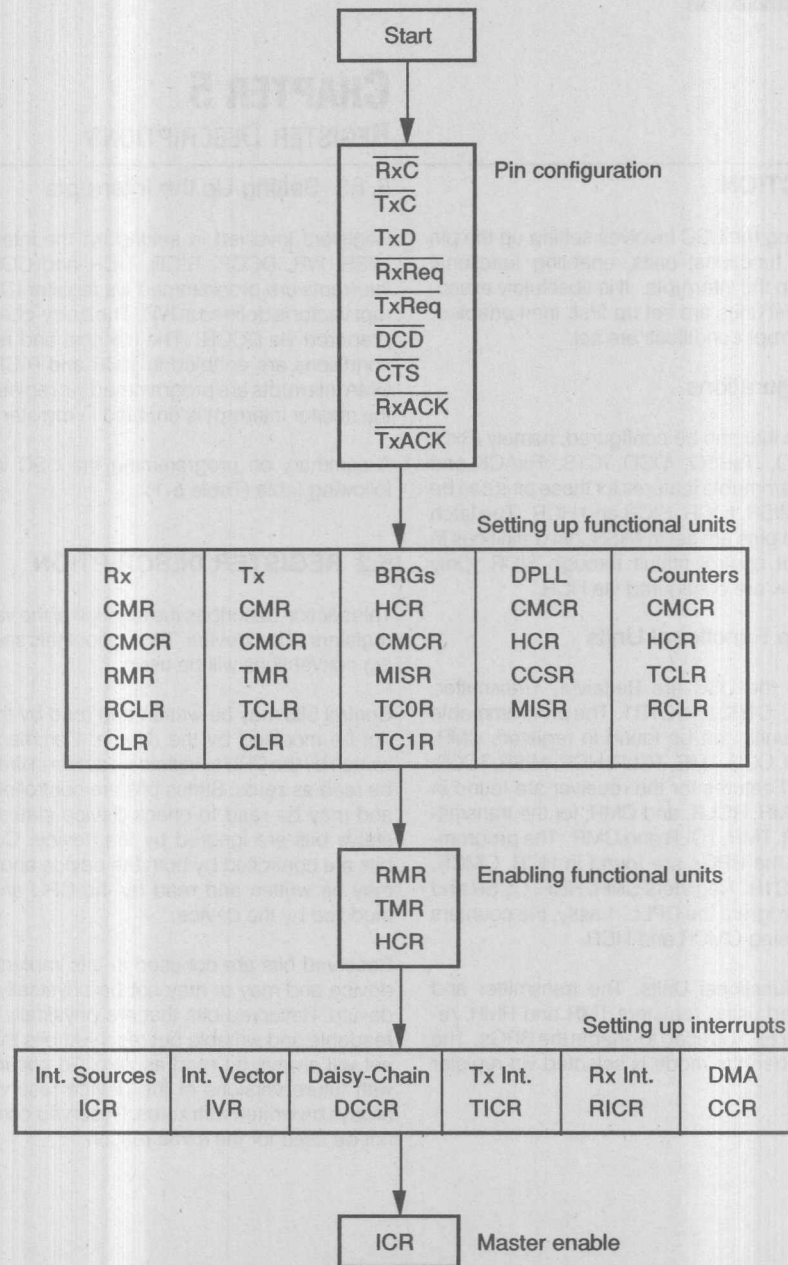


Table 5-2. Register Addressing

Address 43210			Address 43210		
00000	CCAR	Channel Command/Addr Register	10010	RCSR	Receive Command/Status Register
00001	CMR	Channel Mode Register	10011	RICR	Receive Interrupt Control Register
00010	CCSR	Channel Command/Status Register	10100	RSR	Receive Sync Register
00011	CCR	Channel Control Register	10101	RCLR	Receive Count Limit Register
00110	TMDR	Test Mode Data Register	10110	RCCR	Receive Character Count Register
00111	TMCR	Test Mode Control Register	10111	TCOR	Time Constant 0 Register
01000	CMCR	Clock Mode Control Register	1X000	TDR	Transmit Data Register (Write Only)
01001	HCR	Hardware Configuration Register	11001	TMR	Transmit Mode Register
01010	IVR	Interrupt Vector Register	11010	TCSR	Transmit Command/Status Register
01011	IOCR	I/O Control Register	11011	TICR	Transmit Interrupt Control Register
01100	ICR	Interrupt Control Register	11100	TSR	Transmit Sync Register
01101	DCCR	Daisy-chain Control Register	11101	TCLR	Transmit Count Limit Register
01110	MISR	Misc Interrupt Status Register	11110	TCCR	Transmit Character Count Register
01111	SICR	Status Interrupt Control Register	11111	TC1R	Time Constant 1 Register
1X000	RDR	Receive Data Register (Read Only)			
10001	RMR	Receive Mode Register	XXXXX	BCR	Bus Configuration Register

5.3 CHANNEL COMMAND/ADDRESS REGISTER

The upper byte of the Channel Command/Address Register (CCAR) contains command and control fields for the channel. The lower byte of the CCAR serves as an address pointer for the channel.

5.3.1 Channel Command Field

Bits 15 through 11 are encoded with the commands for the channel as shown below:

Bit combination 00000 is a Null command and has no affect on the channel.

Bit combination 00001 is reserved.

Bit combination 00010 is the Reset Highest IUS command. This command resets only the highest priority IUS bit that is set in the channel and occurs independently of the state of the IEI for the channel.

Bit combination 00011 is reserved.

Bit combination 00100 is the Channel Load DMA Trigger command. This command triggers the transmit DMA request for loading the registers in the channel and overrides the function programmed for the /TxREQ pin in the IOCR for the duration of the channel load operation.

During a channel load the DMA transfers addresses and data to the CCAR. The address pointer functions normally

in this mode and either byte or word accesses may be used. If ordinary write cycles are used to write data to the device the data must be written through the CCAR using the address pointer. If the /TxACK signal is used for fly-by transfers to the channel the destination is either the CCAR or the register pointed to by the address pointer in the CCAR.

The channel load operation is terminated when the DMA Continue bit in the CCAR is cleared. Upon termination of the channel load operation the /TxREQ pin will resume the function selected in the IOCR.

Bit combination 00101 is the Receive DMA Trigger command. This command enables the receive DMA request, which is disabled at the end of a frame or message if the Wait for Rx DMA Trigger control bit in the CCR is set to one. It also reloads the receive character counter with the contents of the RCLR.

Bit combination 00110 is the Transmit DMA Trigger command. This command enables the transmit DMA request, which is disabled at the end of a frame or message if the Wait for Tx DMA Trigger control bit in the CCR is set to one. It also reloads the transmit character counter with the contents of the TCLR.

Bit combination 00111 is the Receive and Transmit DMA Trigger command. This command enables both the receive and transmit DMA requests. It also reloads both the receive and transmit character counters.

Bit combination 01000 is reserved.

Address: 00000

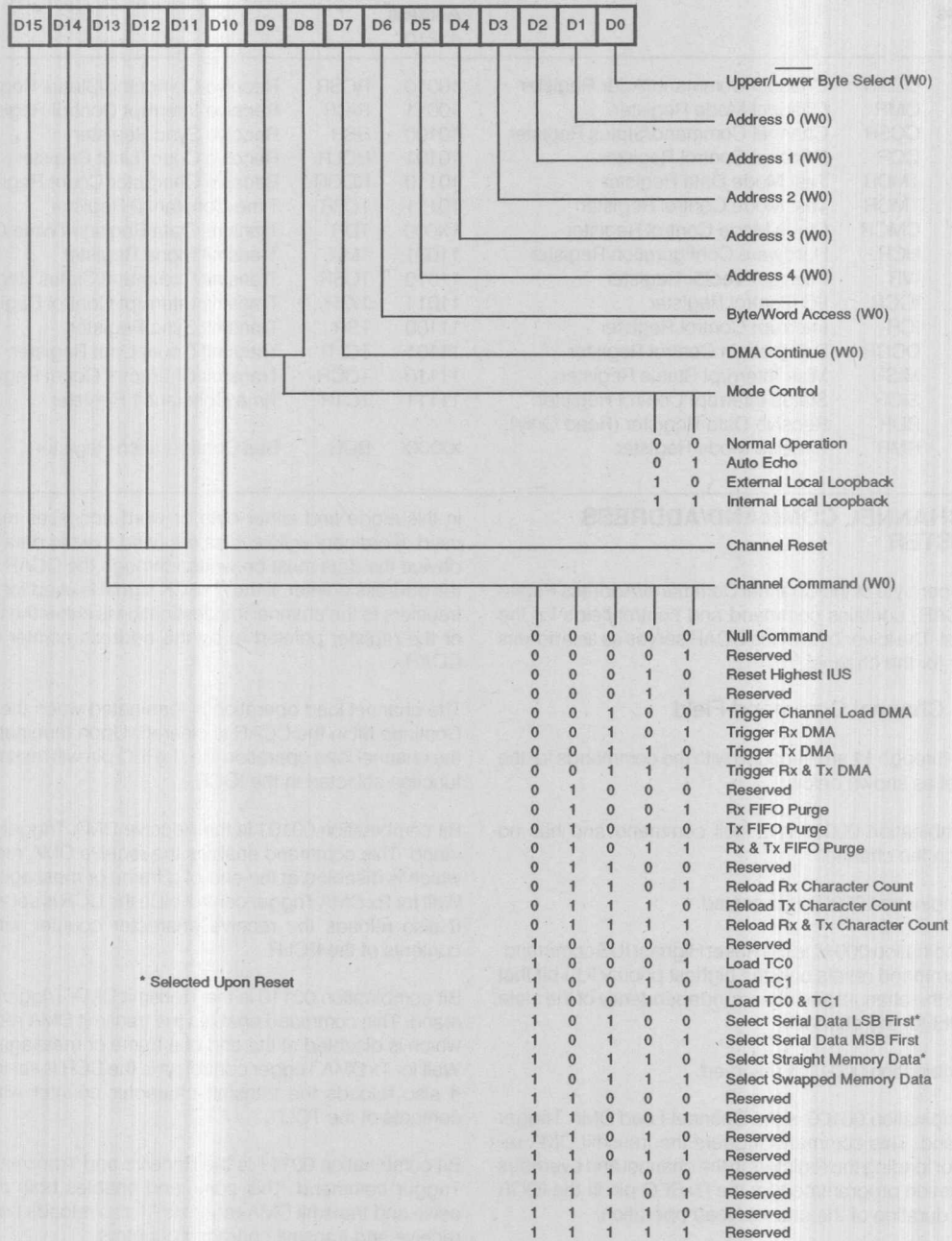


Figure 5-1. Channel Command/Address Register

Bit combination 01001 is the Receive FIFO Purge command. This command removes all entries from the receive FIFO by resetting both the head and tail pointers to zero.

Bit combination 01010 is the Transmit FIFO Purge command. This command removes all entries from the transmit FIFO by resetting both head and tail pointers to zero.

Bit combination 01011 is the Receive and Transmit FIFO purge command. This command removes all entries from both the receive and transmit FIFOs.

Bit combination 01100 is reserved.

Bit combination 01101 is the Reload Receive Character Count command. This command reloads the receive character counter with the contents of the RCLR in preparation for accumulating a new receive character count.

Bit combination 01110 is the Reload Transmit Character Count command. This command reloads the transmit character counter with the contents of the TCLR in preparation for accumulating a new transmit character count.

Bit combination 01111 is the Reload Receive and Transmit Character Count command. This command reloads both the receive character counter and the transmit character counter.

Bit combination 10000 is reserved.

Bit combination 10001 is the Load Time Constant 0 command. This command forces the time constant in the TC0R to be loaded into the counter in BRG0. In single-cycle mode this command also starts the counting operation in BRG0.

Bit combination 10010 is the Load Time Constant 1 command. This command forces the time constant in the TC1R to be loaded into the counter in BRG1. In single-cycle mode this command also starts the counting operation in BRG1.

Bit combination 10011 is the Load Time Constant 0 and Time Constant 1 Command. This command forces the time constant in the TC0R to be loaded into the counter in BRG0 and the time constant in the TC1R to be loaded into the counter in BRG1. In single-cycle mode this command also starts the counting operation in both BRG0 and BRG1.

Bit combination 10100 is the Select Serial Data LSB First command. This command enables the data to be transmit-

ted and received with the least significant bit (bit 0) first. This mode is selected by either hardware or software reset.

Bit combination 10101 is the Select Serial Data MSB First command. This command enables the data to be transmitted and received with the most significant bit (bit 7) first. This selection of bit ordering only applies to the serial data as it enters the transmit FIFO or exits the receive FIFO.

Bit combination 10110 is the Select Straight Memory Data command. This command applies only to the serial data and enables received data read as words to have the byte, which was received first in bits 8 through 15 of the word, and the byte which followed to occupy bits 0 through 7 of the word. Data to be transmitted will be sent bits 8 through 15 first, followed by bits 0 through 7. This mode is selected by either hardware or software reset. Bytes read from the receive FIFO are read in the order that they were received and bytes written to the transmit FIFO are transmitted in the order that they are written to the FIFO.

Bit combination 10111 is the Select Swapped Memory Data command. This command applies only to the serial data and enables received data read as words to have the byte which was received first in bits 0 through 7 of the word, and the byte which followed, to occupy bits 8 through 15 of the word. Data to be transmitted will be sent bits 0 through 7 first, followed by bits 8 through 15. Bytes read from the receive FIFO are read in the order that they were received and bytes written to the transmit FIFO are transmitted in the order that they are written to the FIFO.

Bit combinations 11000 through 11111 are reserved.

5.3.2 Channel Reset Control Bit

Bit 10 is used to reset the channel.

Writing a 0 to this bit has no effect on the channel unless it is in the reset state, at which point the action of writing the 0 removes the channel from the reset state. Note that all zeros must be written to the CCAR to remove the channel from the reset state; it is these zeros that are written to all of the internal registers to give them their reset values.

Setting this bit to 1 forces the channel to enter the reset state, where it will remain until this bit is cleared via another write to the CCAR. All of the registers in the channel are cleared to zero when the channel exits the reset state, but the contents of the registers are undefined while the channel is in the reset state. Note that those bits affecting the pins of the device are cleared directly by the channel reset condition.

5.3.3 Mode Control Field

Bits 9 and 8 select the method for linking for the receiver and transmitter.

Bit combination 00 selects normal, independent operation for the receiver and transmitter.

Bit combination 01 selects the auto echo mode of operation. In this mode any data at the RxD pin is sent to the TxD pin with only gate delays in the path, as well as to the receiver. Any data from the transmitter is lost.

Bit combination 10 selects the TxD pin local loopback mode of operation. In this mode the TxD pin supplies the receive data and any data on the RxD pin is ignored. The TxD pin is still controlled by the TxD Pin Control bits in the IOCR, which allow transmission of the transmit data, to be forced high (1), to forced low (0), or to be 3-state. If the TxD Pin Control bits are set to select a 3-state output, the receiver will sample whatever data is being externally driven on to the TxD pin.

Bit combination 11 selects the internal local loopback mode of operation. In this mode the transmit data is routed directly to the input of the receiver, independent of the state of the TxD Pin Control bits in the IOCR.

5.3.4 DMA Continue Command Bit

Bit 7 is used to control the length of the channel load DMA transfer.

This bit is used only during a channel load DMA transfer and must be set to 1 during the first channel load DMA transfer. This bit is ignored except during the channel load operation. The address pointer written to the CCAR with this bit selects the ultimate destination for the data.

If this bit is set to 1 with the address written during the channel load, the channel load operation continues. In this case, if the address written to the CCAR is neither the word address of the CCAR nor the address of the lower byte of the CCAR, another address data pair will be requested by the channel after the data for this address has been transferred. If the address written to the CCAR is the word address of the CCAR or the address of the lower byte of the CCAR, no data accompanies the address and the next transfer is another address to the CCAR.

If this bit is set to 0 with the address written during the channel load, the channel load operation is terminated and the /TxREQ pin is released to its normal function. In this case, if the address written is the word address of the CCAR or the address of the lower byte of the CCAR, no further transfers are requested, and the pointer is not cleared if pointing to the lower byte of the CCAR. If the

address written is neither the word address of the CCAR, nor the address of the lower byte of the CCAR, another transfer is requested to transfer the data to the addressed register and then the channel load operation is terminated.

5.3.5 Pointer Address Field

Bits 6 through 0 contain the address pointer for the channel.

The address pointer is reset to point to the CCAR by a hardware reset. In the 16-bit bus case, this is 0000000, while in the 8-bit bus case, it is 1000000. Any access of the CCAR actually accesses the register selected by the address pointer. The address pointer is reset to point to the CCAR after this access is complete, which allows the address pointer to be written with another value for the next access.

Reads or writes to registers other than the CCAR, an access of the device with the D//C pin High, signaling data, or an access using the /RxACK or /TxACK pins does not affect the contents of the address pointer except during the channel load operation, where /TxACK selects the CCAR for access.

In the 16-bit bus case, if the pointer is written to point to the lower byte of the CCAR the next read or write will actually be a 16-bit transfer to or from the CCAR. This degenerate case should be avoided. In the 8-bit bus case the Byte/Word bit is forced to indicate byte internally; the user need only indicate upper or lower.

The pointer contains three fields for selecting the register to be accessed; Byte/Word, Address and Upper/Lower. Bit 6 of the pointer selects between byte and word accesses. A word access is selected by a 0 in this bit. This bit is internally forced to 1 when an 8-bit interface is selected for the device. Bits 5 through 1 contain the actual register address. Bit 5 is the most significant bit. Bit 0 controls the selection of the upper or lower byte for a byte access. The lower byte of the register is selected by a 0 in this bit. This bit must be 0 if a word access is selected.

5.4 CHANNEL MODE REGISTER

The Channel Mode register (CMR) contains the mode selection control bits for the channel. The upper byte controls the transmitter, while the lower byte controls the receiver (Figures 5-2 through 5-15).

5.4.1 Transmit Submode Control Field

Bits 15 through 12 are used to select options within each of the main operating modes of the transmitter (Figure 5-2).

In asynchronous mode bits 15 and 14 control the number and type of stop bits for each character, while bits 13 and 12 control the clock rate.

In isochronous mode, bit 14 controls the number of stop bits per character, while bits 15, 13 and 12 are unused.

In async with code violations mode, bits 15 and 14 control the number of stop bits for each character, bit 13 selects the extended word option for 1553B operation, and bit 12 controls the polarity of the code violation pattern used like a start bit.

In monosync mode, bit 15 controls the transmission of CRC when the transmitter underruns, bit 13 enables the transmission of a preamble, bit 12 selects a sync character length other than eight bits and bit 14 is unused.

In bisync mode, bits 15 and 14 control the response of the transmitter to an underrun, bit 13 enables the transmission of a preamble, and bit 12 selects a sync character length other than eight bits.

In HDLC mode, bits 15 and 14 control the response of the transmitter to an underrun, bit 13 enables the transmission of a preamble, and bit 12 enables the transmission of shared-zero flags when the transmitter is idle.

In transparent bisync mode, bits 15 and 14 control the response of the transmitter to an underrun, bit 13 enables the transmission of a preamble, and bit 12 selects the EBCDIC character code instead of the default ASCII.

In NBIP mode, bit 15 controls the polarity of the transmitted address bit, bit 14 enables the transmission of parity on data bytes, while bits 13 and 12 control the clock rate.

In 802.3 mode, bit 15 controls the transmission of CRC when the transmitter underruns and bits 14, 13 and 12 are unused.

In slaved monosync mode, bit 15 controls the transmission of CRC when the transmitter underruns, bit 13 enables the transmitter to go active when the receiver leaves hunt mode, bit 12 selects a sync character length other than eight bits and bit 14 is unused. (See following figures).

In HDLC Loop mode, bits 15 and 14 control the response of the transmitter to an underrun, bit 13 enables the transmitter to go active when the receiver receives a GA sequence, and bit 12 enables the transmission of shared-

zero flags when the transmitter is idle but still active on the loop.

5.4.2 Transmitter Mode Control Field

Bits 11 through 8 are used to select the basic mode of operation for the transmitter.

The transmitter mode should only be changed while the transmitter is disabled and there should be at least one transmit clock between the selection of a new transmit mode and the enable of the transmitter (Figure 5-2).

5.4.2.1 Bit combination 0000 selects Asynchronous mode, where each character is preceded by a start bit of 0 and trailed by some number of stop bits of 1 and the clock is either 16, 32 or 64 times the data rate. The normal idle line condition is all ones (Figure 5-3).

A. In asynchronous mode, Tx Submode bits 3-2 are used to select the number of stop bits to be appended to each character.

Bit combination 00 selects the transmission of one full stop bit.

Bit combination 01 selects the transmission of two full stop bits.

Bit combination 10 selects the transmission of one shaved stop bit. The exact width of the stop bit is controlled by the Tx Shaved Stop Bit Length control field in the CCR.

Bit combination 11 selects the transmission of one full stop bit plus one shaved stop bit. The exact width of the shaved stop bit is controlled by the Tx Shaved Stop Bit Length control field in the CCR.

B. In asynchronous mode, Tx Submode bits 1-0 are used to select the clock divisor rate for the transmitter.

Bit combination 00 selects a transmit clock rate sixteen times the transmit data rate.

Bit combination 01 selects a transmit clock rate thirty-two times the transmit data rate.

Bit combination 10 selects a transmit clock rate sixty-four times the transmit data rate.

Bit combination 11 is reserved.

Address: 00001

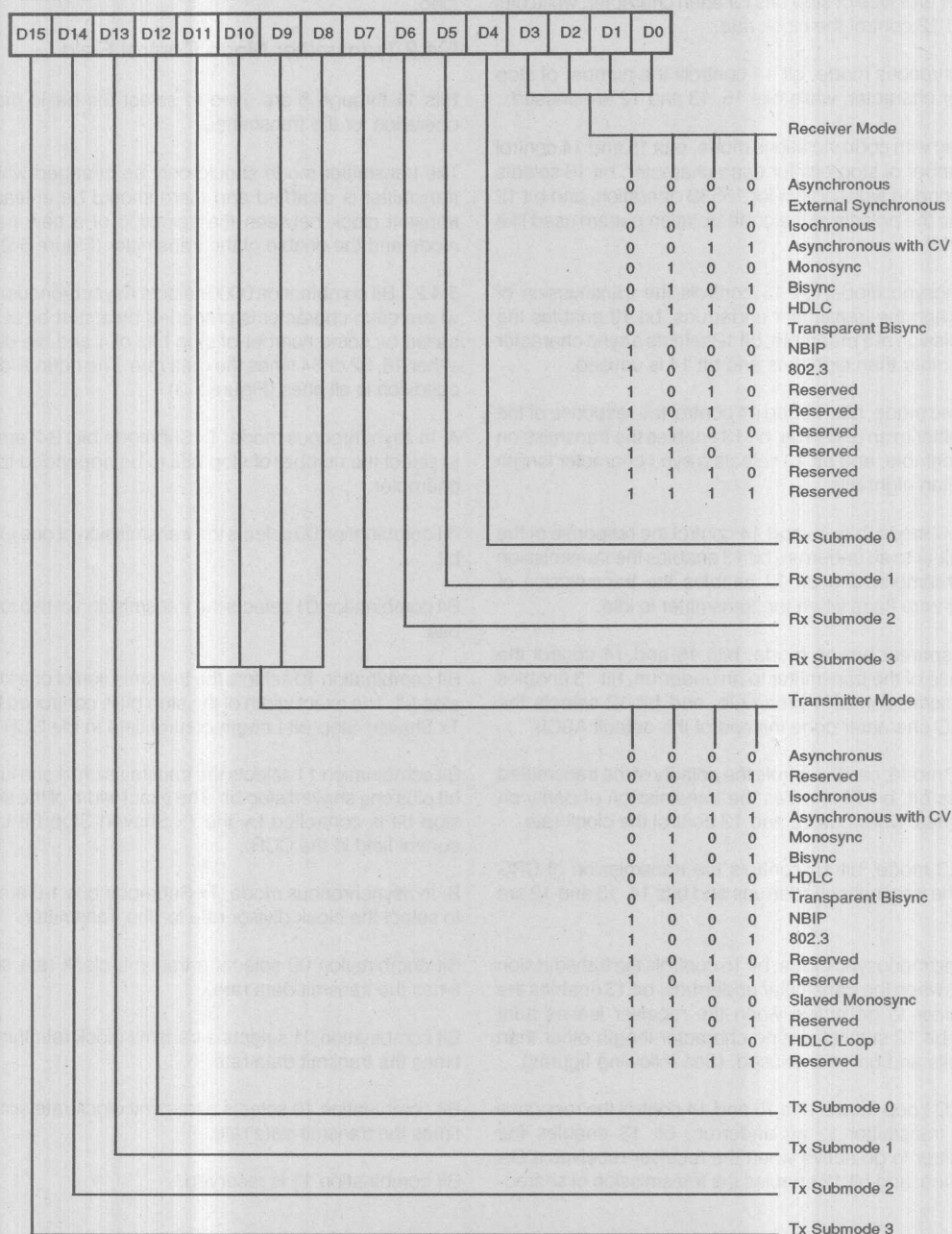


Figure 5-2. Channel Mode Register

Address: 00001

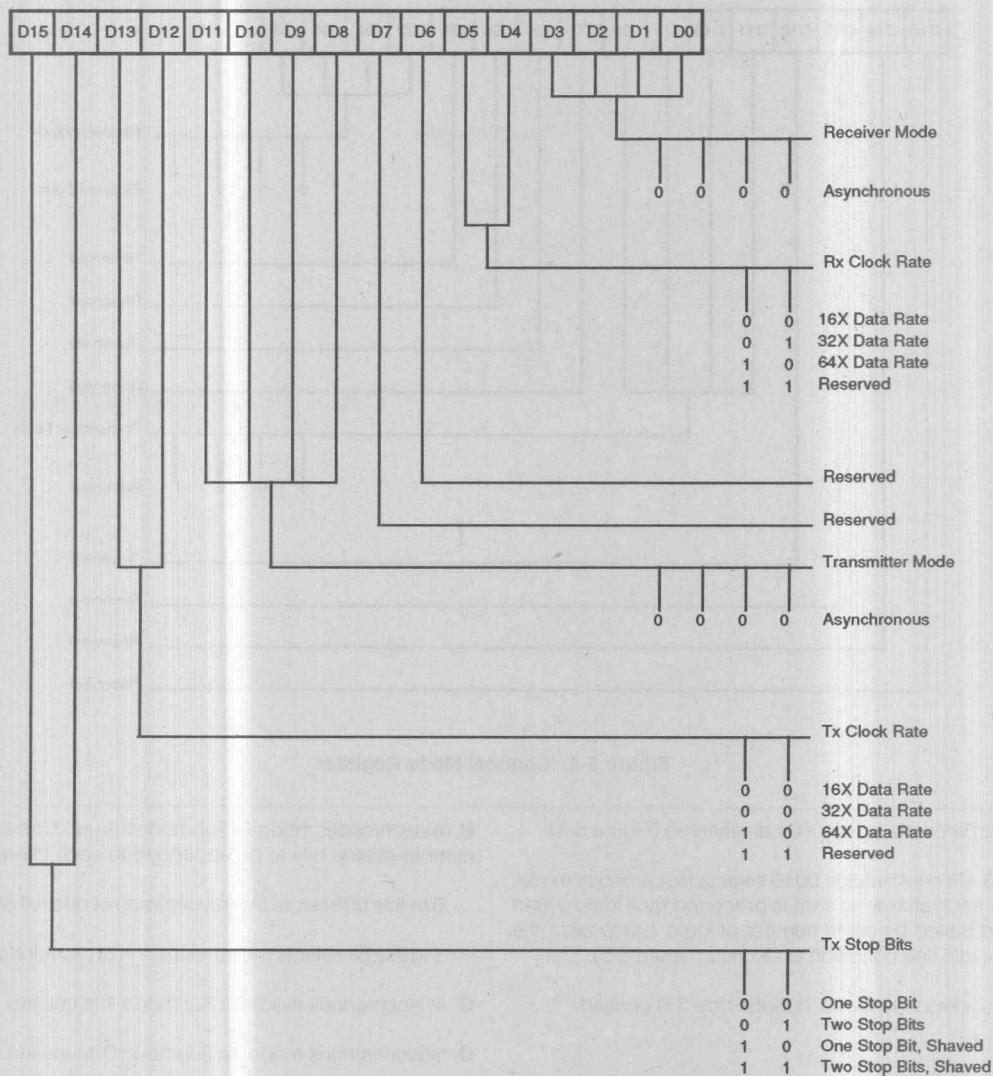


Figure 5-3. Channel Mode Register

Address: 00001

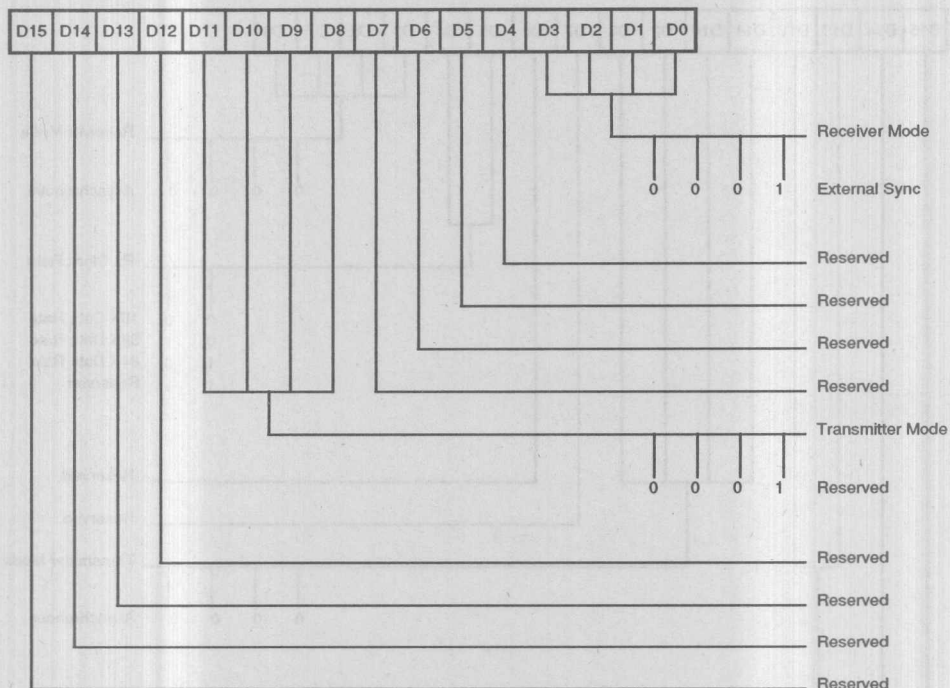


Figure 5-4. Channel Mode Register

5.4.2.2 Bit combination 0001 is reserved (Figure 5-4).

5.4.2.3 Bit combination 0010 selects Isochronous mode, where each character sent is preceded by a logic 0 start bit and trailed by some number of logic 1 stop bits. The normal idle line condition is all ones (Figure 5-5).

A. In isochronous mode Tx Submode 3 is unused.

B. In isochronous mode Tx Submode 2 is used to select the number of stop bits to be appended to each character.

0 in this bit selects the transmission of one full stop bit.

1 in this bit selects the transmission of two full stop bits.

C. In isochronous mode Tx Submode 1 is unused.

D. In isochronous mode Tx Submode 0 is unused.

Address: 00001

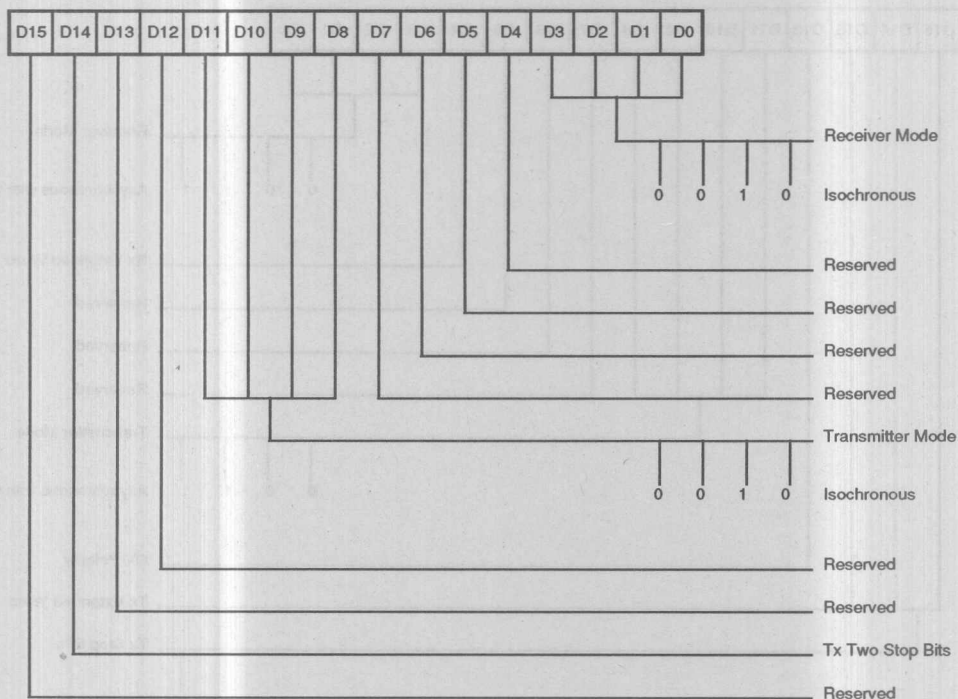


Figure 5-5. Channel Mode Register

5.4.2.4 Bit combination 0011 selects Asynchronous with Code Violation mode, where each character sent is preceded by a code violation pattern sequence that is three bit times long and is potentially trailed by some number of stop bits. The normal idle line condition is all ones (Figure 5-6).

A. In asynchronous with code violation mode, Tx Submode bits 3-2 are used to select the number of stop bits to be appended to each character.

Bit combination 00 selects the transmission of one stop bit.

Bit combination 01 selects the transmission of two stop bits.

Bit combination 10 selects the transmission of no stop bit. This allows characters to be sent back-to-back, separated only by the code violation pattern.

Bit combination 11 is reserved.

B. In asynchronous with code violation mode, Tx Submode bit 1 is used to enable the extended word option.

0 in this bit disables the extended word option. In this case the character length is controlled by the Tx Character Length and Parity Enable bits in the TMR.

1 in this bit enables the extended word option, for use with 1553B format. In this case the character length must be eight bits, with parity enabled, giving a total of 17 bits per word.

C. In asynchronous with code violation mode, Tx Submode bit 0 is used to select the polarity of the transmitted code violation.

Address: 00001

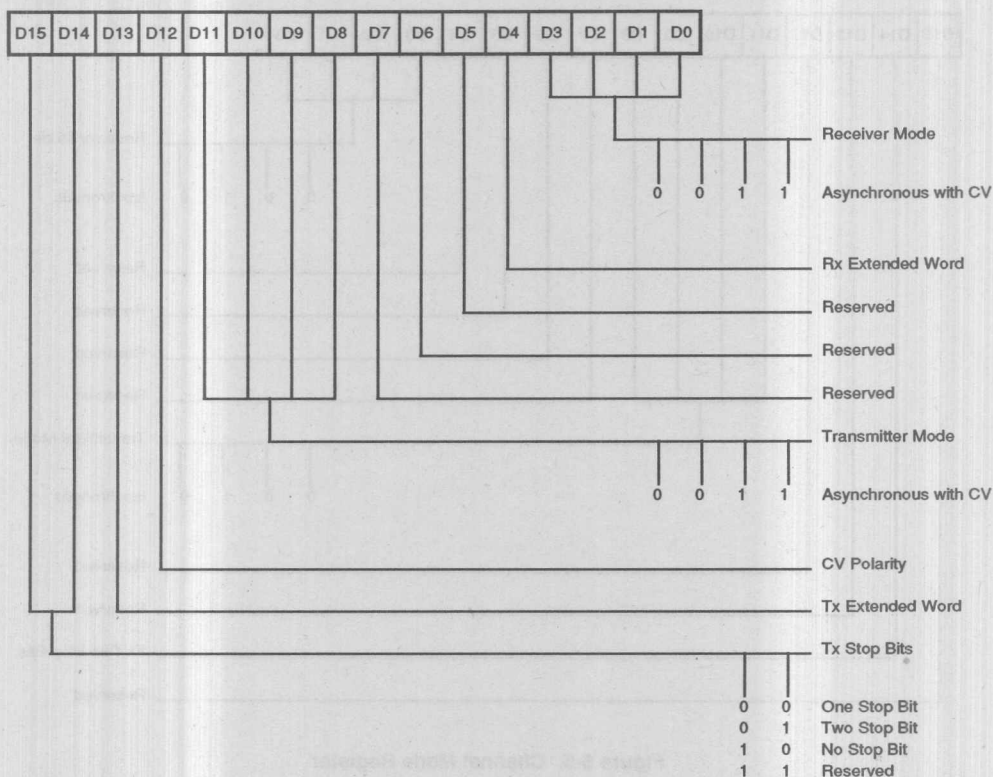


Figure 5-6. Channel Mode Register

D. The state of this bit at the time of the TDR write accompanies the data in the FIFO. Thus the code violation polarity may be changed character by character while still making use of the FIFO. The different code violation waveforms for each of the data encoding formats are shown in Figure 5-7.

0 in this bit selects the "0" code violation pattern, which is the "data" sync signal in 1553B when using biphas-level data encoding.

1 in this bit selects the "1" code violation pattern, which is the "command/status" sync signal in 1553B when using biphas-level data encoding.

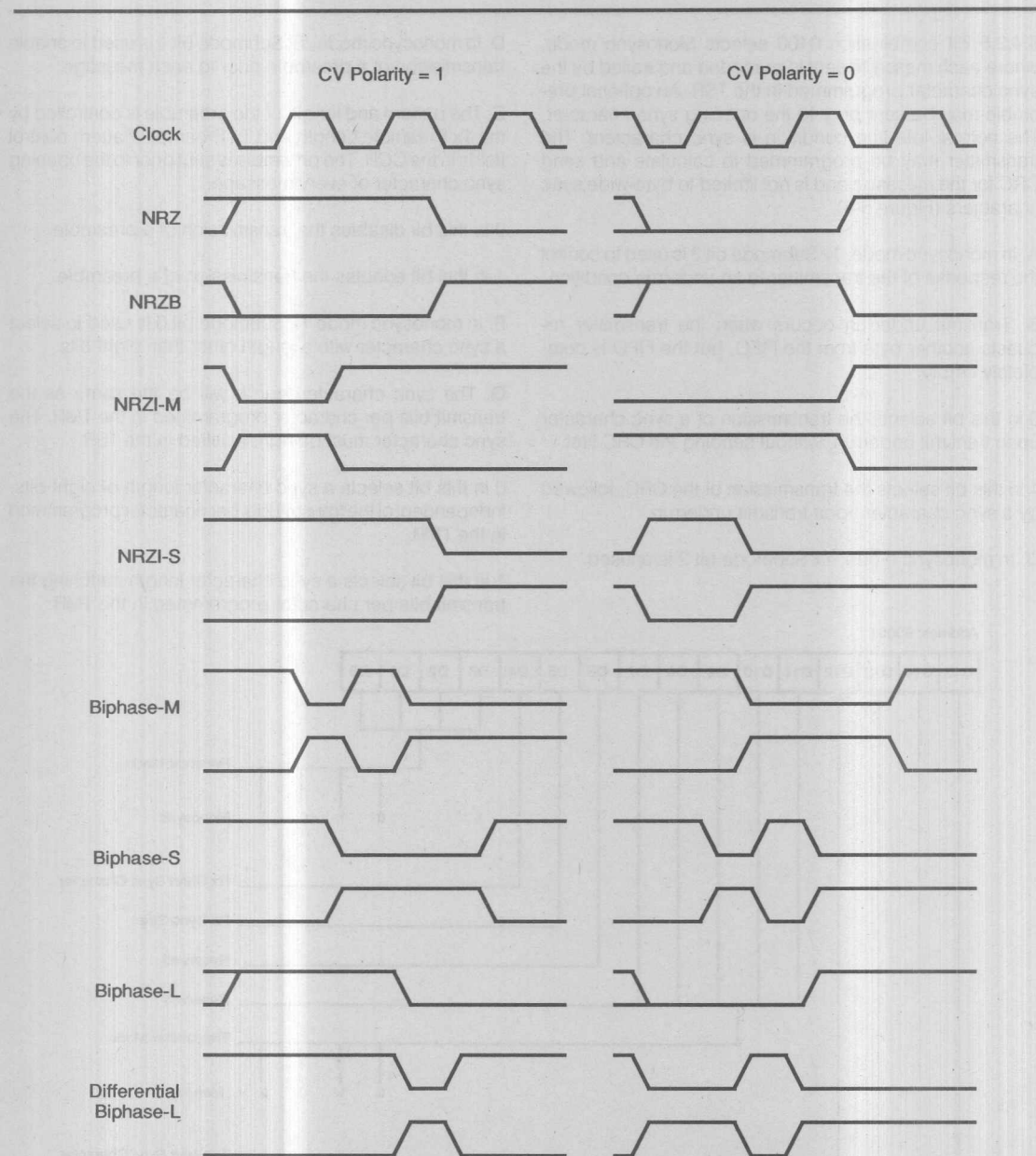


Figure 5-7. Data Encoding Code Violations

5.4.2.5 Bit combination 0100 selects Monosync mode, where each message sent is preceded and trailed by the sync character programmed in the TSR. An optional preamble may be sent prior to the opening sync character. The normal idle line condition is sync characters. The transmitter may be programmed to calculate and send CRC for the message and is not limited to byte-wide sync characters (Figure 5-8).

A. In monosync mode, Tx Submode bit 3 is used to control the response of the transmitter to an underrun condition.

B. Transmit underrun occurs when the transmitter requests another byte from the FIFO, but the FIFO is completely empty.

0 in this bit selects the transmission of a sync character upon transmit underrun, without sending the CRC first.

1 in this bit selects the transmission of the CRC, followed by a sync character upon transmit underrun.

C. In monosync mode, Tx Submode bit 2 is unused.

D. In monosync mode, Tx Submode bit 1 is used to enable transmission of a preamble prior to each message.

E. The pattern and length of the preamble is controlled by the Tx Preamble Length and Tx Preamble Pattern control fields in the CCR. The preamble is sent prior to the opening sync character of every message.

0 in this bit disables the transmission of a preamble.

1 in this bit enables the transmission of a preamble.

F. In monosync mode Tx Submode bit 0 is used to select a sync character with a length other than eight bits.

G. The sync character length will be the same as the transmit bits per character programmed in the TMR. The sync character must be right-justified in the TSR.

0 in this bit selects a sync character length of eight bits, independent of the transmit bits per character programmed in the TMR.

1 in this bit selects a sync character length matching the transmit bits per character programmed in the TMR.

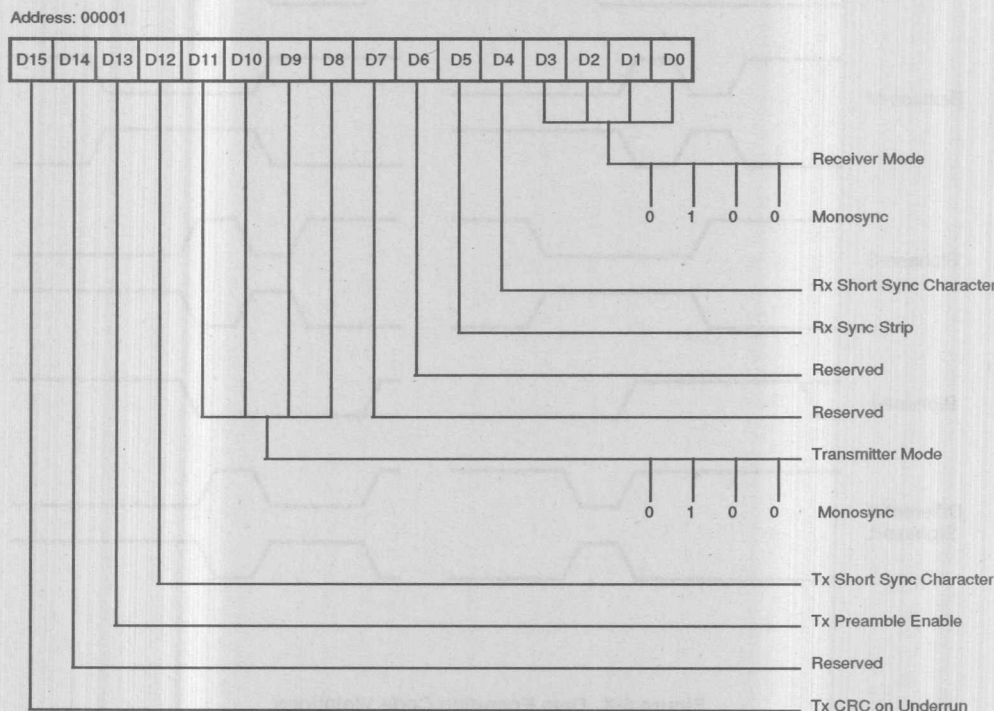


Figure 5-8. Channel Mode Register

5.4.2.6 Bit combination 0101 selects Bisync mode, where each message sent is preceded and trailed by the sync characters programmed in the TSR. An optional preamble may be sent prior to the opening sync character. The normal idle line condition is sync characters. The transmitter may be programmed to calculate and send CRC for the message and is not limited to byte-wide sync characters (Figure 5-9).

A. In bisync mode, Tx Submode bits 3-2 are used to control the response of the transmitter to an underrun condition, as well as the idle line condition.

B. Transmit underrun occurs when the transmitter requests another byte from the FIFO, but the FIFO is completely empty.

Bit combination 00 selects the transmission of the sync character Syn1, held in the upper byte of the TSR, upon underrun. Neither CRC or Syn0 will be sent upon underrun. The idle line condition will be transmission of Syn1 only.

Bit combination 01 selects the transmission of the sync characters Syn0, held in the lower byte of the TSR, and Syn1, held in the upper byte of the TSR, upon underrun. CRC will not be sent upon underrun. The idle line condition will be transmission of Syn0 followed by Syn1, always in pairs.

Bit combination 10 selects the transmission of the CRC and the sync character Syn1, held in the upper byte of the TSR, upon underrun. Syn0 will not be sent upon underrun. The idle line condition will be transmission of Syn1 only.

Bit combination 11 selects the transmission of the CRC and the sync characters Syn0, held in the lower byte of the TSR, and Syn1, held in the upper byte of the TSR, upon underrun. The idle line condition will be transmission of Syn0 followed by Syn1, always in pairs.

C. In bisync mode, Tx Submode bit 1 is used to enable transmission of a preamble prior to each message.

D. The pattern and length of the preamble is controlled by the Tx Preamble Length and Tx Preamble Pattern control fields in the CCR. The preamble is sent prior to the opening sync characters of every message.

0 in this bit disables the transmission of a preamble.

1 in this bit enables the transmission of a preamble.

E. In bisync mode, Tx Submode bit 0 is used to select sync characters with a length other than eight bits.

The sync character length will be the same as the transmit bits per character programmed in the TMR. The sync characters must be right-justified within each byte of the TSR.

0 in this bit selects a sync character length of eight bits, for both sync characters, independent of the transmit bits per character programmed in the TMR.

1 in this bit selects a sync character length matching the transmit bits per character programmed in the TMR for both sync characters.

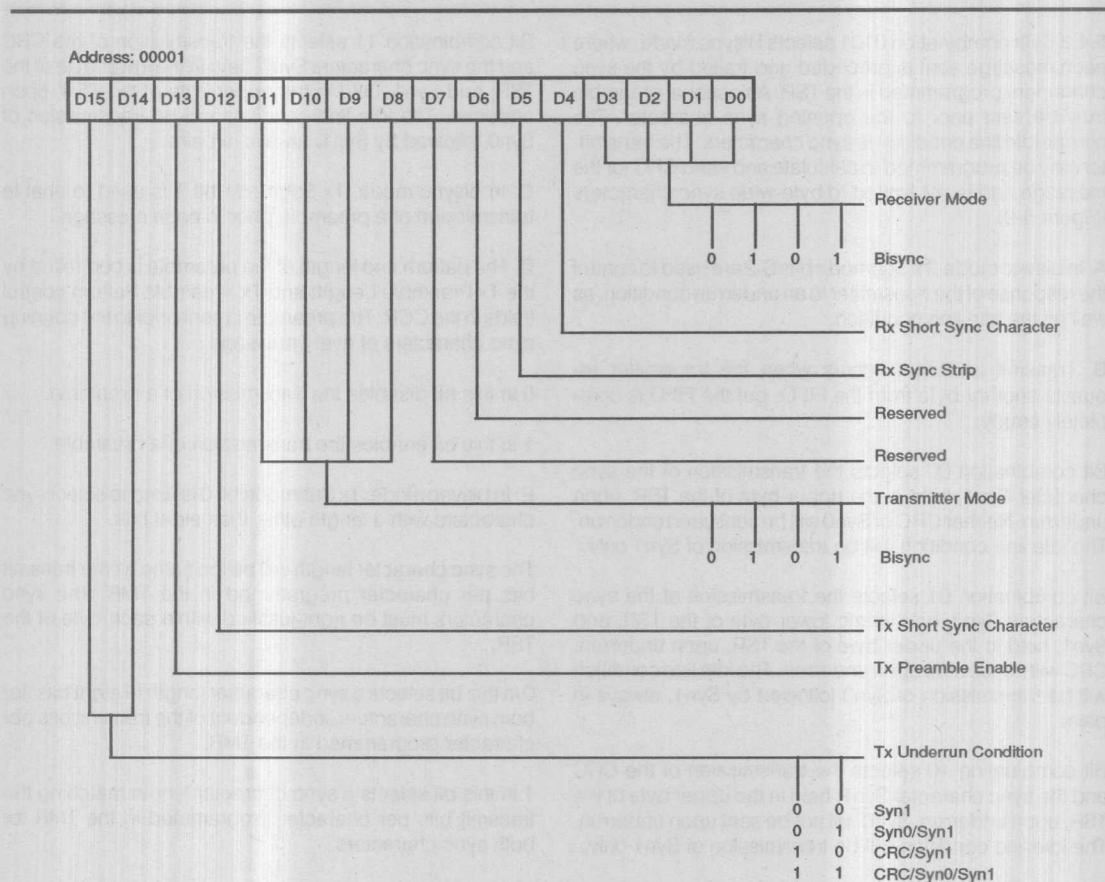


Figure 5-9. Channel Mode Register

5.4.2.7 Bit combination 0110 selects HDLC mode, where each frame sent is preceded and trailed by a unique flag pattern (01111110) and zero insertion is used to ensure data transparency. The normal idle line condition is flags, either with or without shared-zeros. An optional preamble may be sent prior to the opening flag and several options are available for closing the frame (Figure 5-10).

A. In HDLC mode Tx Submode bits 3-2 are used to control the response of the transmitter to an underrun condition.

B. Transmit underrun occurs when the transmitter requests another byte from the FIFO, but the FIFO is completely empty.

Bit combination 00 selects the transmission of an abort upon underrun. The abort is seven consecutive ones, after which the transmitter will send the idle line condition.

Bit combination 01 selects the transmission of an extended abort upon underrun. The extended abort is fifteen consecutive ones, after which the transmitter will send the idle line condition.

Bit combination 10 selects the transmission of a flag only upon underrun, after which the transmitter will send the idle line condition.

Bit combination 11 selects the transmission of the CRC and a flag upon underrun, after which the transmitter will send the idle line condition.

C. In HDLC mode, Tx Submode bit 1 is used to enable transmission of a preamble prior to each message.

D. The pattern and length of the preamble is controlled by the Tx Preamble Length and Tx Preamble Pattern control

fields in the CCR. The preamble is sent prior to the opening sync characters of every message.

0 in this bit disables the transmission of a preamble.

1 in this bit enables the transmission of a preamble.

E. In HDLC mode, Tx Submode bit 0 is used to enable the transmission of shared-zero flags in the normal idle line condition.

F. The opening and closing flags of a frame will never share zeros with idle line flags; even if this bit is set to 1.

0 in this bit disables the transmission of shared-zero flags in the normal idle line condition. That is, the normal idle line will be the pattern 0111111001111110..., with no overlap of flags.

1 in this bit enables the transmission of shared-zero flags in the normal idle line condition. That is, the normal idle line will be the pattern 0111111011111110..., with shared-zero flags.

Address: 00001

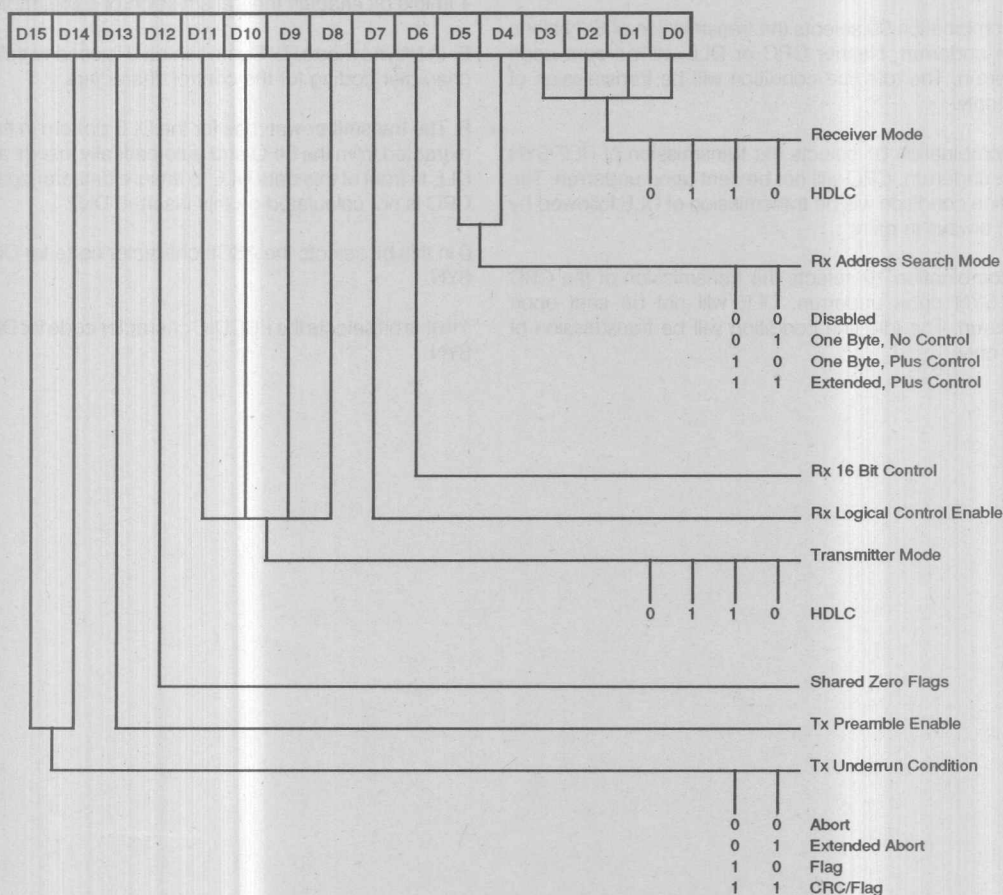


Figure 5-10. Channel Mode Register

5.4.2.8 Bit combination 0111 selects Transparent Bisync mode, where each message sent is preceded by the DLE and SYN characters. An optional preamble may be sent prior to the opening DLE-SYN combination. The normal idle line condition is either DLE-SYN or SYN alone. The transmitter may be programmed to calculate and send CRC for the message (Figure 5-11).

A. In transparent bisync mode Tx Submode bits 3-2 are used to control the response of the transmitter to an underrun condition, as well as the idle line condition.

B. Transmit underrun occurs when the transmitter requests another byte from the FIFO, but the FIFO is completely empty.

Bit combination 00 selects the transmission of SYN alone upon underrun. Neither CRC or DLE will be sent upon underrun. The idle line condition will be transmission of SYN only.

Bit combination 01 selects the transmission of DLE-SYN upon underrun. CRC will not be sent upon underrun. The idle line condition will be transmission of DLE followed by SYN, always in pairs.

Bit combination 10 selects the transmission of the CRC and SYN upon underrun. DLE will not be sent upon underrun. The idle line condition will be transmission of SYN only.

Bit combination 11 selects the transmission of the CRC and DLE-SYN upon underrun. The idle line condition will be transmission of DLE followed by SYN, always in pairs.

C. In transparent bisync mode, Tx Submode bit 1 is used to enable transmission of a preamble prior to each message.

D. The pattern and length of the preamble is controlled by the Tx Preamble Length and Tx Preamble Pattern control fields in the CCR. The preamble is sent prior to the opening sync characters of every message.

0 in this bit disables the transmission of a preamble.

1 in this bit enables the transmission of a preamble.

E. In bisync mode, Tx Submode bit 0 is used to select the character coding for the control characters.

F. The transmitter watches for the DLE pattern in the data extracted from the FIFO and automatically inserts another DLE in front of this data DLE to ensure data transparency. CRC is not calculated on this inserted DLE.

0 in this bit selects the ASCII character code for DLE and SYN.

1 in this bit selects the EBCDIC character code for DLE and SYN.

Address: 00001

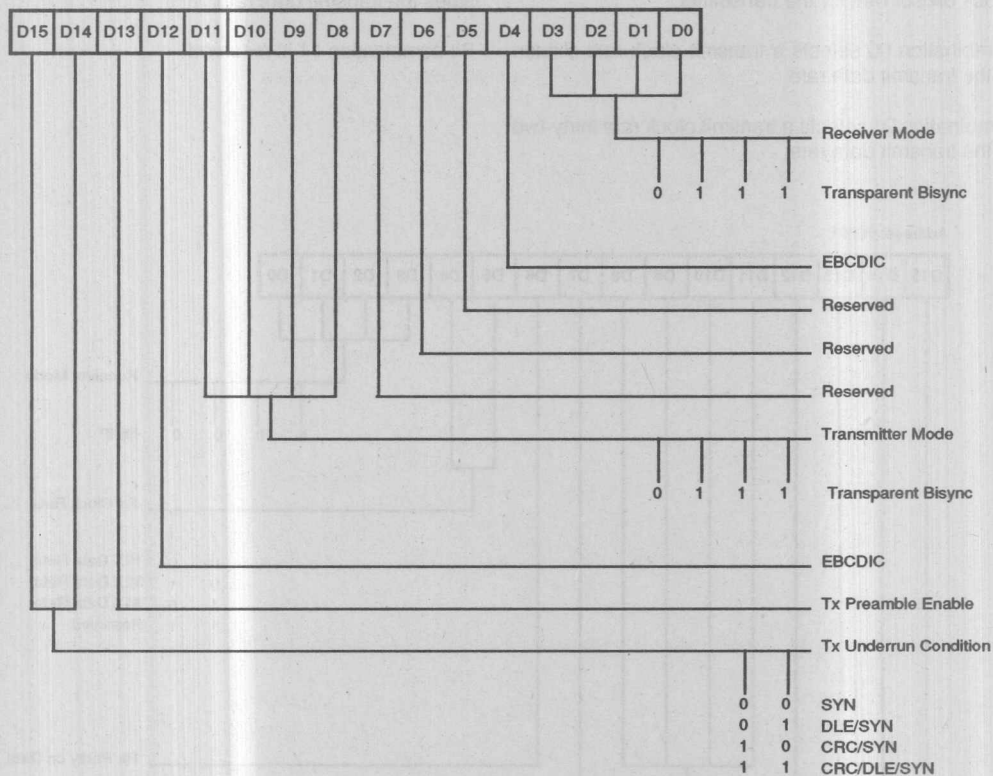


Figure 5-11. Channel Mode Register

5.4.2.9 Bit combination 1000 selects NBIP mode, where each character sent is preceded by a logic 0 start bit and trailed by an address/data bit and a logic 1 stop bits and the clock is either 16, 32 or 64 times the data rate. The normal idle line condition is all ones (Figure 5-12).

A. In NBIP mode, Tx Submode bit 3 is used to select the polarity of the address/data bit transmitted in the ninth bit position.

B. The state of this bit at the time of the TDR write accompanies the data in the FIFO. Thus, the address/data bit polarity may be changed character by character while still making use of the FIFO.

0 in this bit sends a 0 in the ninth bit position, to signal that this is a data byte.

1 in this bit sends a 1 in the ninth bit position, to signal that this is an address byte.

C. In NBIP mode Tx Submode bit 2 is used to enable the inclusion of parity in data characters.

0 in this bit inhibits the inclusion of parity in the eighth bit position for both addresses and data. Thus, eighth bits of data may be sent per byte. Those bytes marked as addresses in the FIFO (using the Tx Address Bit) should be written to the FIFO with the correct parity in the MSB, accounting for the transmitted address bit, since receivers always check parity on received addresses.

1 in this bit enables the inclusion of parity in the eighth bit position. Thus, only seven bits of data may be sent per byte. Note that parity must still be enabled on the TMR.

D. In NBIP mode, Tx Submode bits 1-0 are used to select the clock divisor rate for the transmitter.

Bit combination 00 selects a transmit clock rate sixteen times the transmit data rate.

Bit combination 01 selects a transmit clock rate thirty-two times the transmit data rate.

Bit combination 10 selects a transmit clock rate sixty-four times the transmit data rate.

Bit combination 11 is reserved.

Address: 00001

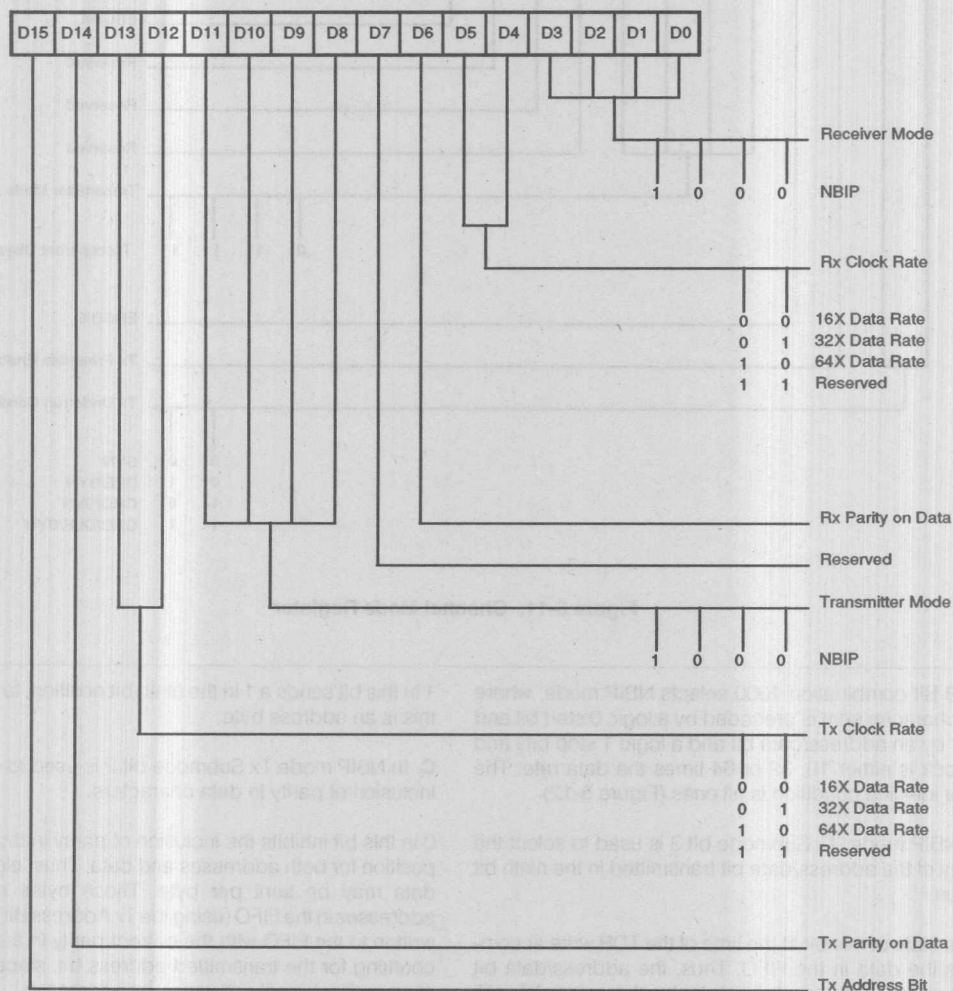


Figure 5-12. Channel Mode Register

5.4.2.10 Bit combination 1001 selects 802.3 mode, where each message is preceded by a preamble and start bit of 1, and is terminated with CRC without any trailing delimiter. To meet the IEEE 802.3 standard, biphas-level data encoding must be programmed in the TMR. An idle line condition of mark or space, selected in the TCSR, will allow external logic to terminate the transmit signal on the physical medium because of the absence of a mid-bit transition. In this mode the /CTS input could then be used to signal a collision detect to the processor and disable the transmitter (Figure 5-2.10).

A. In 802.3 mode, Tx Submode bit 3 is used to control the response of the transmitter to an underrun condition.

B. Transmit underrun occurs when the transmitter requests another byte from the FIFO, but the FIFO is completely empty.

0 in this bit selects the transmission an idle line condition upon transmit underrun, without sending the CRC first.

1 in this bit selects the transmission of the CRC, followed by the idle line condition upon transmit underrun.

C. In 802.3 mode, Tx Submode bit 2 is unused.

D. In 802.3 mode, Tx Submode bit 1 is unused.

E. In 802.3 mode, Tx Submode bit 0 is unused.

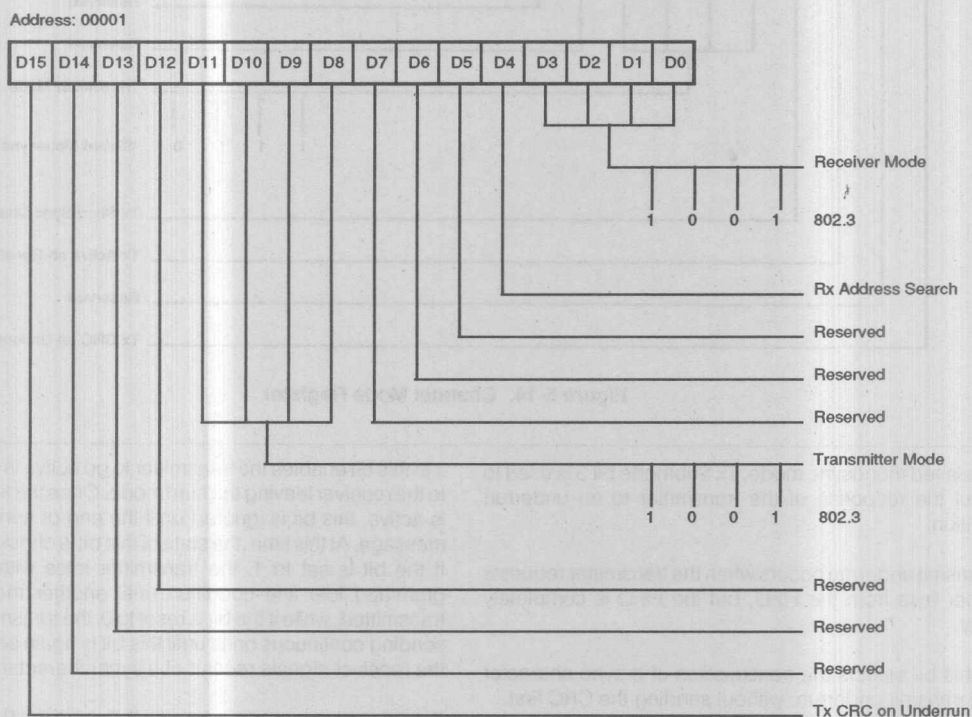


Figure 5-13. Channel Mode Register

5.4.2.11 Bit combinations 1010 and 1011 are reserved.

5.4.2.12 Bit combination 1100 selects Slaved Monosync mode, where the transmitter waits for the receiver to signal that it has left the hunt mode to go active. While inactive the transmitter sends ones and upon activation the data will be sent byte-synchronously with the receive data. Once the transmitter is active, this mode is identical to normal monosync mode, where each message sent is preceded and

trailed by the sync character programmed in the TSR. An optional preamble may be sent prior to the opening sync character and the normal idle line condition is sync characters. The transmitter may be programmed to calculate and send CRC for the message and is not limited to byte-wide sync characters, although byte synchronization will only be achieved in the case of byte-wide sync characters (Figure 5-14).

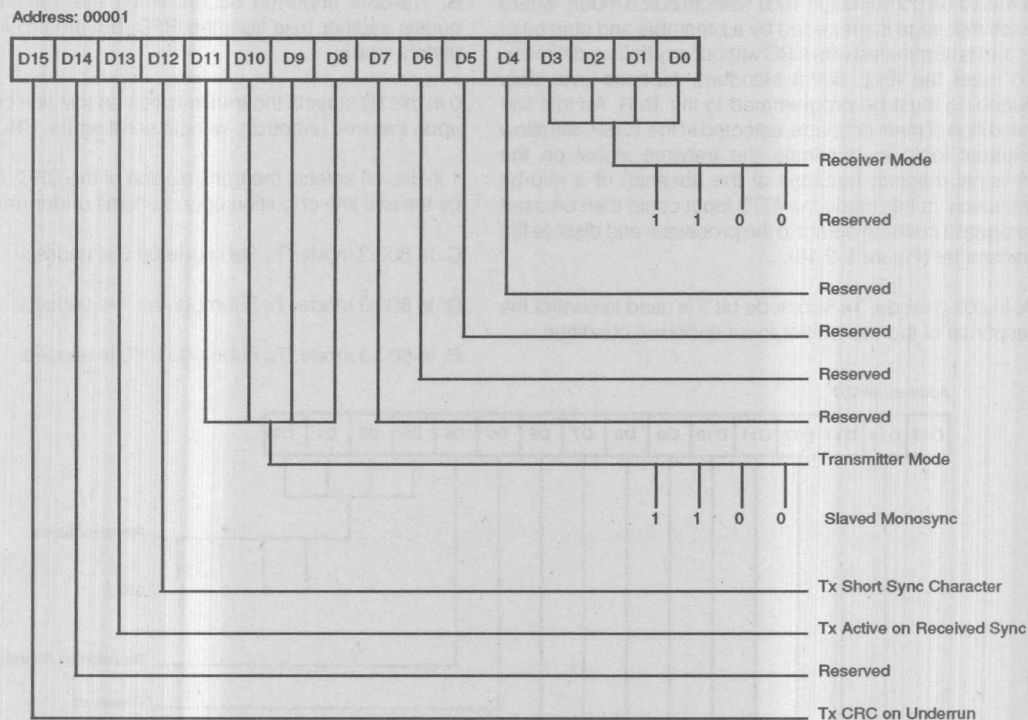


Figure 5-14. Channel Mode Register

A. In slaved monosync mode, Tx Submode bit 3 is used to control the response of the transmitter to an underrun condition.

B. Transmit underrun occurs when the transmitter requests another byte from the FIFO, but the FIFO is completely empty.

0 in this bit selects the transmission of a sync character upon transmit underrun, without sending the CRC first.

1 in this bit selects the transmission of the CRC, followed by a sync character upon transmit underrun.

C. In slaved monosync mode, Tx Submode bit 2 is unused.

D. In slaved monosync mode, Tx Submode bit 1 is used to enable the transmitter to go active when the receiver signals that it has left the hunt mode.

0 in this bit prevents the transmitter from going active at all.

1 in this bit enables the transmitter to go active in response to the receiver leaving the hunt mode. Once the transmitter is active, this bit is ignored until the end of a transmitted message. At this time, the state of this bit is checked again. If the bit is set to 1, the transmitter idles with the programmed idle line condition until another message is transmitted, while if the bit is reset to 0, the transmitter idles sending continuous ones until this bit is again set to 1 and the receiver signals receipt of a sync character.

E. In slaved monosync mode, Tx Submode bit 0 is used to select a sync character with a length other than eight bits.

F. The sync character length will be the same as the transmit bits per character programmed in the TMR. The sync character must be right-justified in the TSR.

0 in this bit selects a sync character length of eight bits, independent of the transmit bits per character programmed in the TMR.

1 in this bit selects a sync character length matching the transmit bits per character programmed in the TMR.

5.4.2.13 Bit combination 1101 is reserved.

5.4.2.14 Bit combination 1110 selects HDLC Loop mode, where the receiver and transmitter are linked to form a repeating station for loop applications. While on loop any received data is echoed via the transmit data pin after a four bit-time delay. Upon receipt of the Go Ahead sequence (01111111), the transmitter may be programmed to change this sequence into a flag sequence (01111110) and start sending one or more frames on the loop. Upon completion of frame transmission, the transmitter reverts to echoing the receive data stream (Figure 5-15).

A. In HDLC Loop mode, Tx Submode bits 3-2 are used to control the response of the transmitter to an underrun condition.

B. Transmit underrun occurs when the transmitter requests another byte from the FIFO, but the FIFO is completely empty.

Bit combination 00 selects the transmission of an abort upon underrun. The abort is seven consecutive ones, after which the transmitter will revert to echoing the receive data. That is, the transmitter stops sending on the loop. Note that if continuous ones are being received at this time, the transmitter will then interpret these ones as a Go Ahead and will begin sending Flags on the loop if the Go Active On Poll bit is set to 1.

Bit combination 01 selects the transmission of an extended abort upon underrun. The extended abort is fifteen consecutive ones, after which the transmitter will revert to echoing the receive data. That is, the transmitter stops sending on the loop. Note that if continuous ones are being received at this time, the transmitter will then interpret these ones as a Go Ahead and will begin sending Flags on the loop if the Go Active On Poll bit is set to 1.

Bit combination 10 selects the transmission of a flag only upon underrun, after which the transmitter will continue to send flags on the loop until either another frame is to be sent or until the Tx Active On Poll bit in this register is set to 0.

Bit combination 11 selects the transmission of the CRC and a flag upon underrun, after which the transmitter will continue to send flags on the loop until either another frame is to be sent or until the Tx Active On Poll bit in this register is set to 0.

C. In HDLC Loop mode Tx Submode bit 1 is used to enable the transmitter to either insert itself in the loop or go active on the loop.

0 in this bit prevents the transmitter from either inserting itself in the loop or going active on the loop.

1 in this bit enables the transmitter to either insert itself in the loop or go active on the loop.

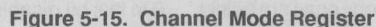
D. When this bit is first set to 1 after the transmitter is enabled, continuous zeros are sent until the Go Ahead (GA) is received. If this bit is set to 1 at that time the transmitter will go on loop, and echo the receive data with a four bit-time delay. Once on loop the transmitter cannot go active until another GA is received with this bit set to 1. When this occurs, the transmitter changes the GA into a flag and begin frame transmission. The transmitter sends on the loop until either this bit is reset to 0 or until an abort is sent by the transmitter.

E. In HDLC Loop mode, Tx Submode bit 0 is used to enable the transmission of shared-zero flags in the normal idle line condition.

F. The opening and closing flags of a frame will never share-zeros with idle line flags; even if this bit is set to 1.

0 in this bit disables the transmission of shared-zero flags in the normal idle line condition. That is, the normal idle line will be the pattern 0111111001111110..., with no overlap of flags.

1 in this bit enables the transmission of shared-zero flags in the normal idle line condition. That is, the normal idle line will be the pattern 0111111011111110..., with shared-zero flags.



In transparent bisync mode, bit 12 selects the EBCDIC character code instead of the default ASCII and bits 7, 6 and 5 are unused.

In NBIP mode, bit 6 enables the checking of parity on data bytes, bits 5 and 4 control the clock rate and bit 7 is unused.

In 802.3 mode, bit 4 enables the address match logic, while bits 7, 6 and 5 are unused.

5.4.4 Receiver Mode Control Field

Bits 3 through 0 are used to select the basic mode of operation for the receiver.

The receiver mode should only be changed while the receiver is disabled and there should be at least one receive clock between the selection of a new receive mode and the enable of the receiver.

5.4.4.1 Bit combination 0000 selects Asynchronous mode, where each character received is preceded by a start bit of 0 and trailed by a stop bit of 1 and the clock is either 16, 32 or 64 times the data rate.

A. In asynchronous mode, Rx Submode bit 3 is unused.

B. In asynchronous mode, Rx Submode bit 2 is unused.

C. In asynchronous mode, Rx Submode bits 1-0 are used to select the clock divisor rate for the receiver.

Bit combination 00 selects a receive clock rate sixteen times the receive data rate.

Bit combination 01 selects a receive clock rate thirty-two times the receive data rate.

Bit combination 10 selects a receive clock rate sixty-four times the receive data rate.

Bit combination 11 is reserved.

5.4.4.2 Bit combination 0001 selects External Sync mode, where an external sync signal is used to establish character synchronization. In this mode the receiver merely assembles the data, checking parity and CRC if so programmed, after receiving the sync signal. Character assembly is stopped when the sync signal is removed. In this mode the /DCD pin must be programmed to act as a DCD/ SYNC input in the IOCR. When the sync signal is removed, the character being assembled is completed and transferred to the FIFO before the receiver stops the character assembly process. Timing for /SYNC is shown in Figure 5-16.

A. In external sync mode, Rx Submode bit 3 is unused.

B. In external sync mode, Rx Submode bit 2 is unused.

C. In external sync mode, Rx Submode bit 1 is unused.

D. In external sync mode, Rx Submode bit 0 is unused.

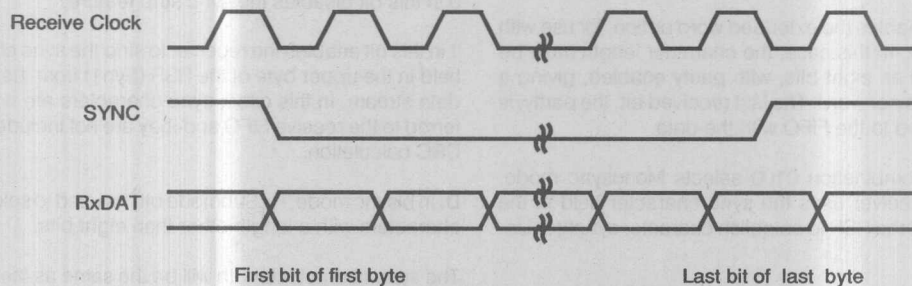


Figure 5-16. Timing for /SYNC

5.4.4.3 Bit combination 0010 selects isochronous mode, where each character received is preceded by a logic 0 start bit and trailed by a logic 1 stop bit.

- A. In isochronous mode, Rx Submode bit 3 is unused
- B. In isochronous mode, Rx Submode bit 2 is unused.
- C. In isochronous mode, Rx Submode bit 1 is unused.
- D. In isochronous mode, Rx Submode bit 0 is unused.

5.4.4.4 Bit combination 0011 selects Asynchronous with Code Violation mode, where each character received is preceded by a code violation pattern sequence that is three bit times long and is potentially trailed by some number of stop bits. Note that the receiver does not check for the presence of the stop bits.

- A. In asynchronous with code violation mode, Rx Submode bit 3 is unused.
- B. In asynchronous with code violation mode, Rx Submode bit 2 is unused.
- C. In asynchronous with code violation mode, Rx Submode bit 1 is unused.
- D. In asynchronous with code violation mode, Rx Submode bit 0 is used to enable the extended word option.

0 in this bit disables the extended word option. In this case the character length is controlled by the Rx Character Length and Parity Enable bits in the RMR.

1 in this bit enables the extended word option, for use with 1553B format. In this case, the character length must be programmed as eight bits, with parity enabled, giving a total of 17 bits per word. The last received bit, the parity, is not transferred to the FIFO with the data.

5.4.4.5 Bit combination 0100 selects Monosync mode, where the receiver uses the sync character held in the upper byte of the RSR to establish character synchronization.

- A. In monosync mode, Rx Submode bit 3 is unused.
- B. In monosync mode, Rx Submode bit 2 is unused.
- C. In monosync mode, Rx Submode bit 1 is used to enable the sync strip logic in the receiver.

0 in this bit disables the sync strip feature.

1 in this bit enables the receiver to strip sync characters from the receive data stream. In this case, sync characters are not transferred to the receive FIFO and they are not included in the CRC calculation.

D. In monosync mode, Rx Submode bit 0 is used to select a sync character with a length other than eight bits.

E. The sync character length will be the same as the receive bits per character programmed in the RMR. The sync character must be right-justified in the RSR with the most significant bit of the sync character duplicated in the high-order bits.

0 in this bit selects a sync character length of eight bits, independent of the receive bits per character programmed in the RMR.

1 in this bit selects a sync character length matching the receive bits per character programmed in the RMR.

5.4.4.6 Bit combination 0101 selects Bisync mode, where the receiver uses the two sync characters held in the RSR to establish character synchronization. The lower byte of the RSR holds Syn0, which is received first, while the upper byte of the RSR holds Syn1, which is received second.

- A. In bisync mode, Rx Submode bit 3 is unused.
- B. In bisync mode, Rx Submode bit 2 is unused.

C. In bisync mode, Rx Submode bit 1 is used to enable the sync strip logic in the receiver.

0 in this bit disables the sync strip feature.

1 in this bit enables the receiver to strip the sync character held in the upper byte of the RSR (Syn1) from the receive data stream. In this case, sync characters are not transferred to the receive FIFO and they are not included in the CRC calculation.

D. In bisync mode, Rx Submode bit 0 is used to select sync characters with a length other than eight bits.

The sync character length will be the same as the receive bits per character programmed in the RMR. The sync characters must be right-justified in each byte of the RSR with the most significant bit of each sync character duplicated in the high-order bits of that byte.

0 in this bit selects a sync character length of eight bits, independent of the receive bits per character programmed in the RMR.

1 in this bit selects a sync character length matching the receive bits per character programmed in the RMR.

5.4.4.7 Bit combination 0110 selects HDLC mode, where each frame received is preceded and trailed by a unique flag pattern (01111110) and zero insertion is used to ensure data transparency.

A. In HDLC mode, Rx Submode bit 3 is used to enable the receiver to recognize logical control fields in the data stream.

B. A logical control field, if present, is a multiple of eight bits at the start of a frame immediately after the address and ordinary control fields. The logical control field is extended, eight bits at a time, if the most significant bit of the byte is a 1. Bytes in the logical control field, if enabled, are transferred to the receive FIFO eight bits at a time, irrespective of the character length selected in the RMR. All subsequent data is transferred to the FIFO using the character length selected in the RMR.

0 in this bit disables the logical control field option.

1 in this bit enables the logical control field option. Logical control fields must be further enabled using bit combination 11 in the Rx Submode 1-0 field in this register.

C. In HDLC mode, Rx Submode bit 2 is used to select the length of the ordinary control field in the data stream.

D. An ordinary control field, if present, is one or two bytes at the start of a frame immediately after the address. Bytes in this control field, if enabled, are transferred to the receive FIFO eight bits at a time, irrespective of the character length selected in the RMR. Subsequent data not in the logical control field is transferred to the FIFO using the character length selected in the RMR.

0 in this bit selects a control field one byte in length.

1 in this bit selects a control field two bytes long. Control fields must be further enabled using bit combination 11 or 10 in the Rx Submode 1-0 field in this register.

E. In HDLC mode, Rx Submode bits 1-0 are used to control the address, compare logic in the receiver, and enable the control field option.

Bit combination 00 disables the address recognition logic in the receiver. All received frames, regardless of address, will be transferred to the receive FIFO. The receiver will transfer all data in the frame to the FIFO using the character length specified in the RMR.

Bit combination 01 enables the address recognition logic in the receiver, with a one byte address field and no control fields. If the address of the frame matches either the address held in the lower byte of the RSR or the global address (all 1's), the frame will be transferred to the receive FIFO. The address byte will be transferred to the FIFO as a byte, with all other data in the frame transferred using the character length specified in the RMR.

Bit combination 10 enables the address recognition logic in the receiver, with a one byte address field and control fields. If the address of the frame matches either the address held in the lower byte of the RSR or the global address (all 1's) the frame will be transferred to the receive FIFO. The address byte will be transferred to the FIFO as a byte, as will the selected control fields, with all other data in the frame transferred using the character length specified in the RMR.

Bit combination 11 enables the address recognition logic in the receiver, with an extended address field and control fields. If the address of the frame matches either the address held in the lower byte of the RSR or the global address (all 1's) the frame will be transferred to the receive FIFO. The address field is extended, eight bits at a time, if the least significant bit of the byte is a 0. Bytes in the selected control fields are transferred to the FIFO as bytes, with all other data in the frame transferred using the character length specified in the RMR.

5.4.4.8 Bit combination 0111 selects Transparent Bisync mode, where the character pair SYN-SYN is used to establish character synchronization and a message is started with either DLE-SOH or DLE-STX. During the message itself, DLEs inserted by the transmitter to ensure data transparency are automatically removed by the receiver and CRC is calculated properly. The message is closed with either DLE-ITB, DLE-ETX, DLE-ETB, DLE-EOT or DLE-ENQ.

A. In bisync transparent mode, Rx Submode 3 is unused.

B. In bisync transparent mode, Rx Submode 2 is unused.

C. In bisync transparent mode, Rx Submode 1 is unused.

D. In bisync mode, Rx Submode bit 0 is used to select the character coding for the control characters.

0 in this bit selects the ASCII character code for DLE and SYN.

1 in this bit selects the EBCDIC character code for DLE and SYN.

5.4.4.9 Bit combination 1000 selects NBIP mode, where each character received is preceded by a logic 0 start bit and trailed by an address/data bit and a logic 1 stop bits and the clock is either 16, 32 or 64 times the data rate.

A. In NBIP mode, Rx Submode bit 3 is unused.

B. In NBIP mode, Rx Submode bit 2 is used to enable the checking of parity on data characters.

0 in this bit inhibits the parity check logic for bytes marked as data. Thus, eight bits of data may be sent per byte. Those bytes marked as addresses are always checked for parity.

1 in this bit enables the parity check logic for bytes marked as data. Thus, only seven bits of data may be sent per byte. Note that parity must still be enabled on the TMR.

C. In NBIP mode, Rx Submode bits 1-0 are used to select the clock divisor rate for the receiver.

Bit combination 00 selects a receive clock rate sixteen times the receive data rate.

Bit combination 01 selects a receive clock rate thirty-two times the receive data rate.

Bit combination 10 selects a receive clock rate sixty-four times the receive data rate.

Bit combination 11 is reserved.

5.4.4.10 Bit combination 1001 selects 802.3 mode, where each message received is preceded by a preamble and start bit of 1, and is terminated with CRC without any trailing delimiter. To meet the IEEE 802.3 standard, biphas-level data encoding must be programmed in the RMR. In this mode the /DCD input is used as a sync signal to delimit the end of a message and disable the receiver. The /DCD pin must be programmed to act as a DCD/SYNC input in the IOCR. When the sync signal is removed the character being assembled is completed and transferred to the FIFO before the receiver stops the character assembly process.

A. In 802.3 mode, Rx Submode bit 3 is unused.

B. In 802.3 mode, Rx Submode bit 2 is unused.

C. In 802.3 mode, Rx Submode bit 1 is unused.

D. In 802.3 mode, Rx Submode bit 0 is used to control the address compare logic in the receiver.

0 in this bit disables the address recognition logic in the receiver. All received frames, regardless of address, will be transferred to the receive FIFO.

1 in this bit enables the address recognition logic in the receiver, with a two byte address field. If the address of the message matches either the address held in the RSR or the global address (all 1's), the frame will be transferred to the receive FIFO.

5.4.4.11 Bit combinations 1010 through 1111 are reserved.

5.5 CHANNEL COMMAND/STATUS REGISTER

The Channel Command/Status register (CCSR) contains miscellaneous command and status bits for the channel (Figure 5-17).

5.5.1 Receive Character Count FIFO Overflow Status Bit

Bit 14 reports the overflow status of the receive character count FIFO.

This bit is always zero unless the receive character count FIFO has overflowed and may be reset to zero by the RCC FIFO Clear command in this register.

This bit is set to 1 and latched when the receive character count FIFO overflows. The receive character count FIFO is four words deep so the receipt of more than four complete frames or messages without read of the RCCR will cause the Receive Character Count FIFO to overflow.

5.5.2 Receive Character Count FIFO Valid Status Bit

Bit 14 reports the status of the receive character count FIFO.

This bit is set to 0 unless the receive character count FIFO contains a valid entry. The RCC FIFO Clear command in this register, thus sets this bit to 0.

This bit is set to 1 if the receive character count FIFO contains at least one valid entry. The top entry in the RCC FIFO may then be read via the RCCR.

5.5.3 Receive Character Count FIFO Clear Command Bit

Bit 13 is a command to clear the receive character count FIFO.

Writing a 1 to this bit clears the receive character count FIFO and the RCC FIFO Valid and RCC FIFO Overflow bits.

5.5.4 DPLL In Sync/Quick Sync Command/Status Bit

Bit 12 reports the synchronization status of the DPLL.

This bit is set to 1 when the DPLL has achieved synchronization with the receive data stream. Writing a 1 to this bit forces the DPLL to lose synchronization and search the incoming data stream for an edge to synchronize to (quick sync mode).

This bit is set to 0 while the DPLL is attempting to synchronize with the receive data stream. Writing a 0 to this bit has no effect on the DPLL (Figure 5-17).

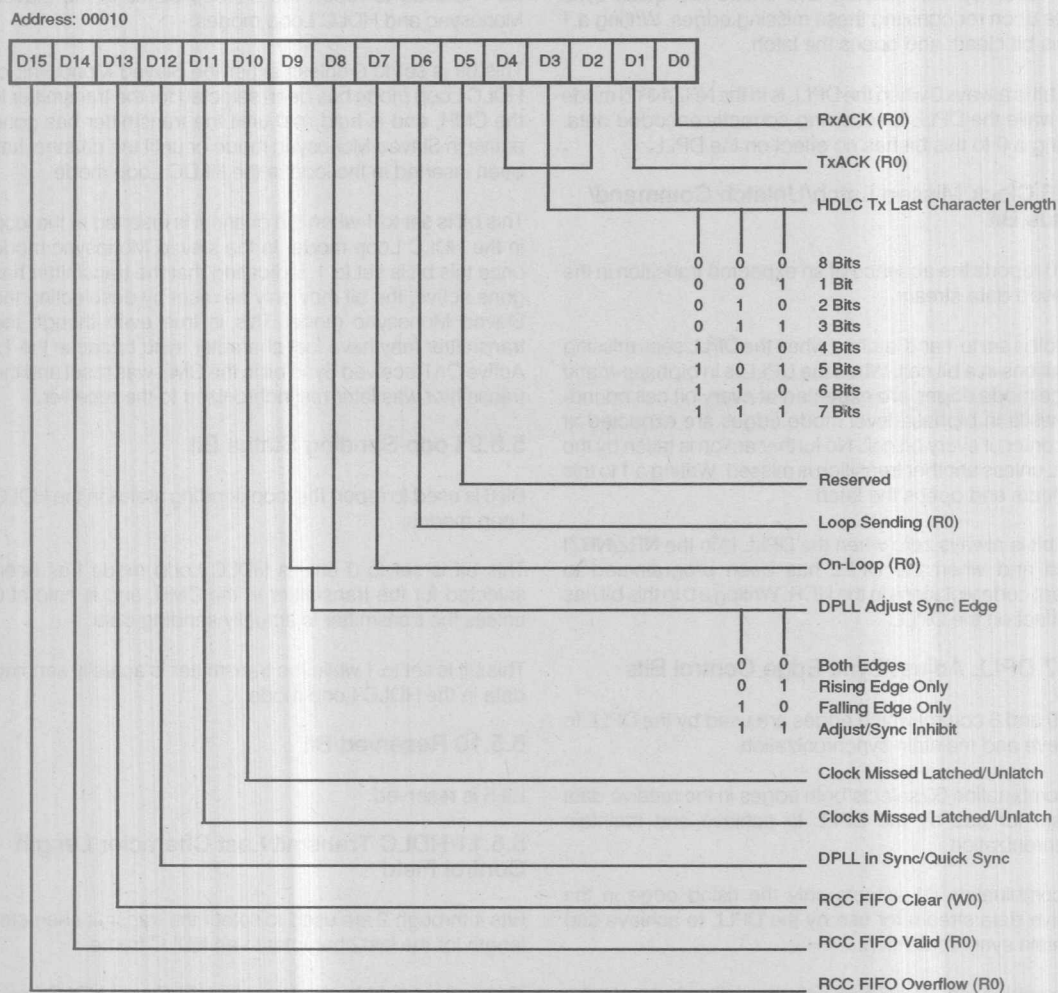


Figure 5-17. Channel Command/Status Register

5.5.5 Clocks Missed Latch/Unlatch Command/Status Bit

Bit 11 reports the absence of an expected transition in two consecutive bit cells in the received data stream.

This bit is set to 1 and latched when the DPLL sees missing transitions in two successive bit cells. When the DPLL is in biphase-mark/space mode edges are expected at every bit cell boundary, while in biphase-level mode edges are expected at the center of every bit cell. The DPLL automatically loses synchronization and enters the quick sync mode upon recognizing these missing edges. Writing a 1 to this bit clears and opens the latch.

This bit is always 0 when the DPLL is in the NRZ/NRZI mode and while the DPLL is receiving correctly encoded data. Writing a 0 to this bit has no effect on the DPLL.

5.5.6 Clock Missed Latch/Unlatch Command/Status Bit

Bit 10 reports the absence of an expected transition in the received data stream.

This bit is set to 1 and latched when the DPLL sees missing transitions in a bit cell. When the DPLL is in biphase-mark/space mode edges are expected at every bit cell boundary, while in biphase-level mode edges are expected at the center of every bit cell. No further action is taken by the DPLL unless another transition is missed. Writing a 1 to this bit clears and opens the latch.

This bit is always zero when the DPLL is in the NRZ/NRZI mode and when the DPLL has been programmed to accept code violations in the HCR. Writing a 0 to this bit has no effect on the DPLL.

5.5.7 DPLL Adjust/Sync Edge Control Bits

Bits 9 and 8 control which edges are used by the DPLL to achieve and maintain synchronization.

Bit combination 00 selects both edges in the receive data stream for use by the DPLL to achieve and maintain synchronization.

Bit combination 01 selects only the rising edge in the receive data stream for use by the DPLL to achieve and maintain synchronization.

Bit combination 10 selects only the falling edge in the receive data stream for use by the DPLL to achieve and maintain synchronization.

Bit combination 11 inhibits the DPLL from using either edge in the receive data stream to achieve and maintain synchronization.

As far as the DPLL is concerned, edges that may not be used to achieve or maintain synchronization are not present and will be reported as missing edges when they occur where an edge is expected.

5.5.8 On-Loop Status Bit

Bit 7 is used to report the on-loop status in the Slaved Monosync and HDLC Loop modes.

This bit is set to 0 unless either the Slaved Monosync or HDLC Loop mode has been selected for the transmitter in the CMR, and is held at 0 until the transmitter has gone active in Slaved Monosync mode or until the channel has been inserted in the loop in the HDLC Loop mode.

This bit is set to 1 when the channel is inserted in the loop in the HDLC Loop mode. In the slaved Monosync mode once this bit is set to 1, indicating that the transmitter has gone active, the bit may only be reset by deselecting the Slaved Monosync mode. This is true even though the transmitter may have lost character sync because the Tx Active On Received Sync bit in the CMR was reset and the transmitter was later resynchronized to the receiver.

5.5.9 Loop Sending Status Bit

Bit 6 is used to report the loop sending status in the HDLC Loop modes.

This bit is set to 0 unless HDLC Loop mode has been selected for the transmitter in the CMR, and is held at 0 unless the transmitter is actually sending data.

This bit is set to 1 while the transmitter is actually sending data in the HDLC Loop mode.

5.5.10 Reserved Bit

Bit 5 is reserved.

5.5.11 HDLC Transmit Last Character Length Control Field

Bits 4 through 2 are used to select the transmit character length for the last character in an HDLC frame.

This control field is used only in HDLC and HDLC Loop modes; and then only for the character marked with EOF, which is the last character in a transmitted frame. The data

bits must be right-justified in the TDR. Note that if parity is enabled, the parity bit will be sent in addition to the number of bits programmed for the last character. This is not the same as ordinary data, which has the parity bit included in the programmed character length.

Bit combination 000 selects a character length of eight bits.

Bit combination 001 selects a character length of one bit.

Bit combination 010 selects a character length of two bits.

Bit combination 011 selects a character length of three bits.

Bit combination 100 selects a character length of four bits.

Bit combination 101 selects a character length of five bits.

Bit combination 110 selects a character length of six bits.

Bit combination 111 selects a character length of seven bits.

5.5.12 TxACK Status Bit

Bit 1 is used to report the state of the /TxACK pin.

This bit is set to 0 unless the /TxACK pin has been programmed to be a 3-state output in the HCR and reflects the complemented state of the /TxACK pin, if this pin has been programmed to be a 3-state output in the HCR.

5.5.13 RxACK Status Bit

Bit 1 is used to report the state of the /RxACK pin.

This bit is set to 0 unless the /RxACK pin has been programmed to be a 3-state output in the HCR and reflects the complemented state of the /RxACK pin, if this pin has been programmed to be a 3-state output in the HCR.

5.6 CHANNEL CONTROL REGISTER

The Channel Control register (CCR) contains additional mode control bits for the channel. The upper byte controls the transmitter, while the lower byte controls the receiver (Figure 5-18).

Address: 00011

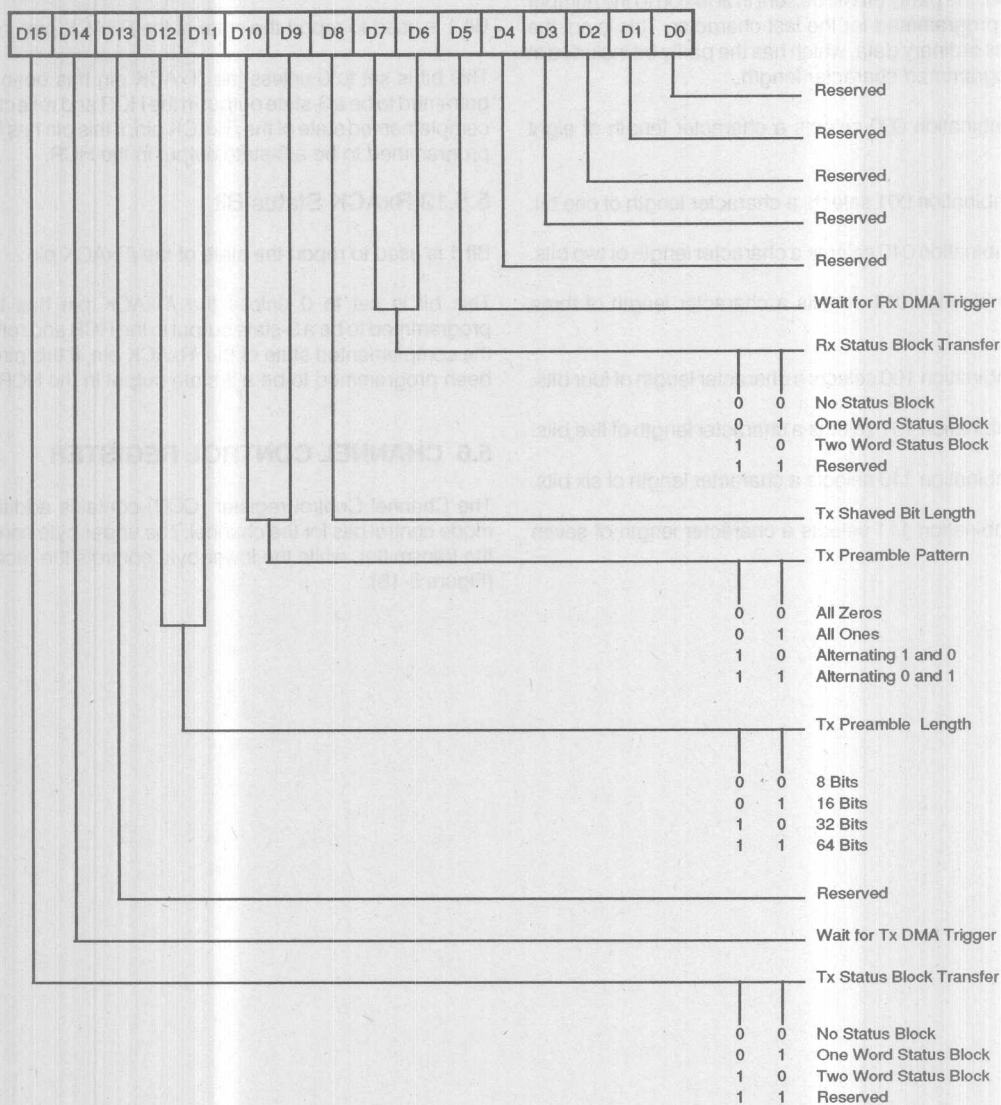


Figure 5-18. Channel Control Register

5.6.1 Transmit Status Block Transfer Control Field

Bits 15 and 14 are used to control any transmit status block transfer.

The transmit status block consists of one or two words of control information, pertaining to the message to be transmitted, that are transferred to the device as if they were data in advance of the actual data to be transmitted.

The first word of the transmit status block, though written as data to the address of the TDR, is actually written to the TSBR. The second word of the transmit status block, though written as data to the address of the TDR, is written to the TCLR.

If a transmit status block transfer is enabled, the first data written to the address of the TDR after a Transmit DMA Trigger, Reload Transmit Character Count or Transmit FIFO Purge command is the transmit status block. Likewise, after the transmit character counter has decremented to a count of zero, the next data written to the address of the TDR is the transmit status block.

Bit combination 00 disables the transmit status block option. In this case all data written to the address of the TDR is destined for the TDR.

Bit combination 01 selects a transmit status block consisting of one word. This word is written to the TSBR.

Bit combination 10 selects a transmit status block consisting of two words. The first word is written to the TSBR and the second word is written to the TCLR.

Bit combination 11 is reserved.

5.6.2 Wait For Transmit DMA Trigger Control Bit

Bit 13 is used to control DMA requests at the end of a transmitted frame or message.

0 in this bit enables DMA requests to continue (transferring data for the next frame or message) after the last byte of a transmit frame or message is written to the transmit FIFO.

1 in this bit inhibits DMA requests at the end of a transmitted frame or message until a Trigger Transmit DMA command is issued in the CCAR. This is true even if the transmit FIFO is empty beyond the level programmed for DMA requests in the TICR.

5.6.3 Reserved Bit

Bit 12 is reserved.

5.6.4 Transmit Preamble Length Control Field

Bits 11 and 10 are used to select the length of the preamble in all synchronous modes.

The transmitter sends the preamble, if enabled, in advance of the first flag or sync character in a message.

Bit combination 00 selects a preamble length of 8-bits.

Bit combination 01 selects a preamble length of 16-bits.

Bit combination 10 selects a preamble length of 32-bits.

Bit combination 11 selects a preamble length of 64-bits.

5.6.5 Transmit Preamble Pattern Control Field

Bits 9 and 8 are used to select the bit pattern of the preamble in all synchronous modes.

Bit combination 00 selects a preamble pattern of all zeros for the programmed length.

Bit combination 01 selects a preamble pattern of all ones for the programmed length.

Bit combination 10 selects a preamble pattern of alternating ones and zeros, ending with a zero, for the programmed length.

Bit combination 11 selects a preamble pattern of alternating ones and zeros, ending with a one, for the programmed length.

5.6.6 Transmit Shaved Stop Bit Length Control Field

Bits 11 through 8 are used to select the length of a shaved stop bit in asynchronous mode.

A value of "n" in this field selects $(n+1)/16$ of a bit-time for the shaved stop bit length.

5.6.7 Receive Status Block Transfer Control Field

Bits 7 and 6 are used to control any receive status block transfer.

The receive status block consists of one or two words of status information that are transferred from the device as if they were data at the end of a received frame or message. After the transfer of the character marked with the CV/EOT/EOF status bit, the next one or two reads of the RDR transfer the receive status block.

If the receive status block is enabled, the first word, though read as data from the address of the RDR, is actually read from the RSBR, while the second word of the receive status block, if used, is actually read from the RCHR.

Bit combination 00 disables the receive status block option. In this case all data read from the address of the RDR actually comes from the RDR.

Bit combination 01 selects a receive status block consisting of one word. This word is read from the RSBR.

Bit combination 10 selects a receive status block consisting of two words. The first word is read from the RSBR and the second word is read from the RCHR.

Bit combination 11 is reserved.

5.6.8 Wait For Receive DMA Trigger Control Bit

Bit 4 is used to control DMA requests at the end of a received frame or message.

0 in this bit enables DMA requests to continue (transferring data for the next frame or message) after the last byte of a received frame or message is read from the receive FIFO.

1 in this bit inhibits DMA requests at the end of a received frame or message until a Trigger Receive DMA command is issued in the CCAR. This is true even if the receive FIFO is full beyond the level programmed for DMA requests in the RICR.

5.6.9 Reserved Bits

Bits 4 through 0 are reserved.

5.7 PRIMARY RESERVED REGISTER

The Primary Reserved Register (PRR) is not used in this implementation of the device. Any data written to this register will be ignored and zeros will always be read in this register (Figure 5-19).

Address: 00100

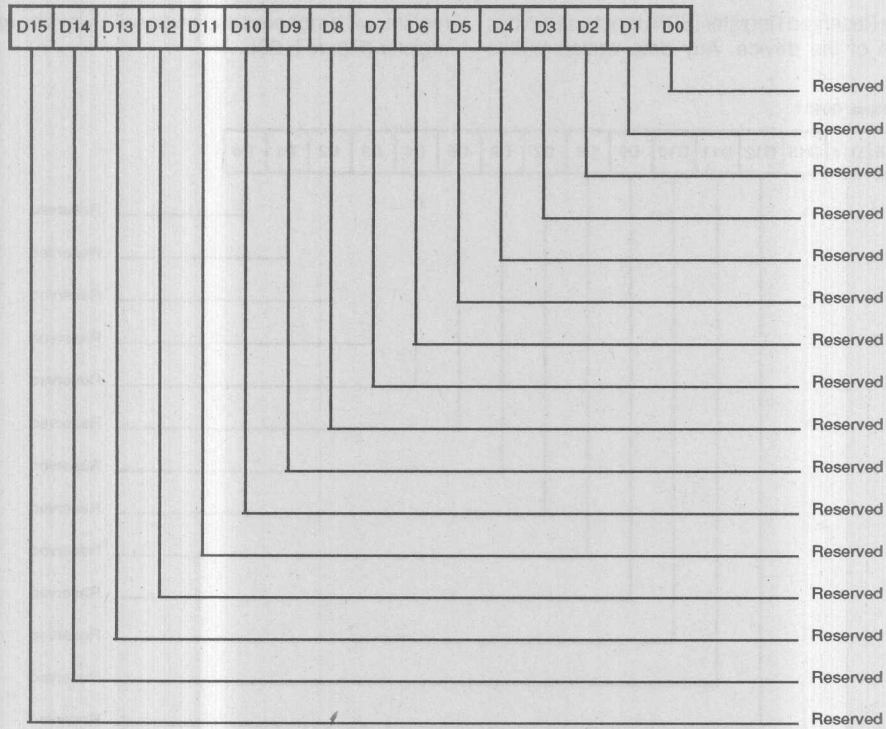


Figure 5-19. Primary Reserved Register

Address: 00110

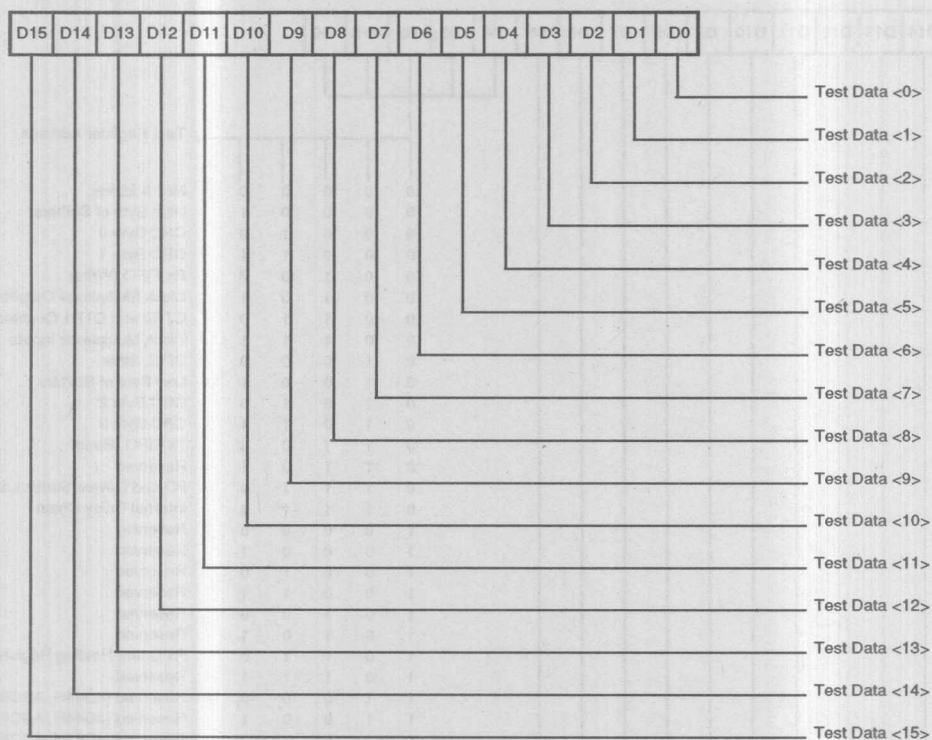
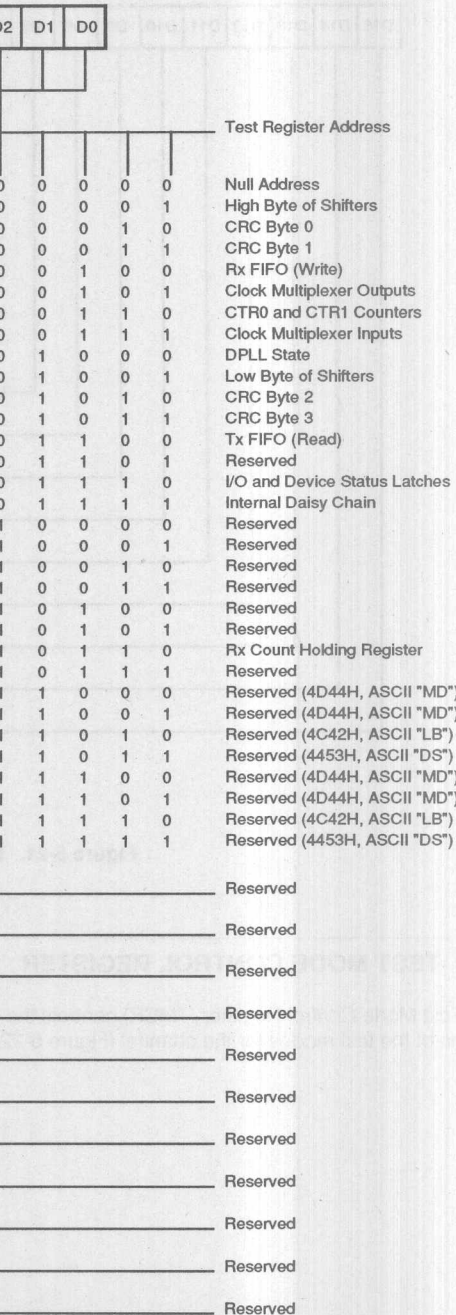


Figure 5-21. Test Mode Data Register

5.10 TEST MODE CONTROL REGISTER

The Test Mode Control Register (TMCR) controls the operation of the test modes for the channel (Figure 5-22).



Control Register

5.10.1 Reserved Bits

Bits 15 through 5 are reserved and should not be used. Any data written to these bits will be ignored and zeros will always be read in these bit locations.

5.10.2 Test Register Address Control Field

Bits 4 through 0 are used as an address to select a set of internal signals to be accessed through the TMDR. Once written, this address remains valid until written with a different value. All test registers, except for the Rx FIFO and the I/O and Device Status Latches, are read-only.

Bit combination 00000 is the null address.

Bit combination 00001 selects the high byte of the transmit and receive shift registers for access through the TMDR.

Bit combination 00010 selects byte 0 of the transmit and receive CRC registers for access through the TMDR.

Bit combination 00011 selects byte 1 of the transmit and receive CRC registers for access through the TMDR.

Bit combination 00100 selects the bottom of the receive FIFO for access through the TMDR. This test register is write-only. The bottom of the receive FIFO should only be written while the receive clock is High, after which the receive clock should be pulsed Low to perform the actual write to the FIFO.

Bit combination 00101 selects the output of the clock multiplexer for access through the TMDR.

Bit combination 00110 selects the counters of CTR0 and CTR1 for access through the TMDR.

Bit combination 00111 selects the input to the clock multiplexer for access through the TMDR.

Bit combination 01000 selects the internal state of the DPLL for access through the TMDR.

Bit combination 01001 selects the low byte of the transmit and receive shift registers for access through the TMDR.

Bit combination 01010 selects byte 2 of the transmit and receive CRC registers for access through the TMDR.

Bit combination 01011 selects byte 3 of the transmit and receive CRC registers for access through the TMDR.

Bit combination 01100 selects the top of the transmit FIFO for access through the TMDR. The transmit clock must be High during this access and then must be pulsed Low to move the read pointer in the FIFO and extract the data.

Bit combination 01101 is reserved and should not be used.

Bit combination 01110 selects the I/O and device status interrupt latches for access through the TMDR. This test register is write only.

Bit combination 01111 selects the state of the internal daisy-chain for access through the TMDR.

Bit combinations 10000 through 10101 are reserved and should not be used.

Bit combination 10110 selects the Receive Count Holding Register for access through the TMDR.

Bit combinations 10111 through 11111 are reserved.

5.11 CLOCK MODE CONTROL REGISTER

The Clock Mode Control register (CMCR) contains control fields which select the sources of clock signals for the various blocks within the channel (Figure 5-23).

5.11.1 CTR1 Clock Source Control Field

Bits 15 and 14 are used to select the source of the clock for CTR1.

Bit combination 00 is used to disable CTR1. The internal state of the counter is reset to all zeros while it is disabled.

Bit combination 01 is used to disable CTR1. The internal state of the counter is reset to all zeros while it is disabled.

Bit combination 10 selects the /RxC pin as the clock source for CTR1.

Bit combination 11 selects the /TxC pin as the clock source for CTR1.

5.11.2 CTR0 Clock Source Control Field

Bits 13 and 12 are used to select the source of the clock for CTR0.

Bit combination 00 is used to disable CTR0. The internal state of the counter is reset to all zeros while it is disabled.

Bit combination 01 is used to disable CTR0. The internal state of the counter is reset to all zeros while it is disabled.

Bit combination 10 selects the /RxC pin as the clock source for CTR0.

Bit combination 11 selects the /TxC pin as the clock source for CTR0.

5.11.3 BRG1 Clock Source Control Field

Bits 11 and 10 are used to select the source of the clock for BRG1. The clock source for BRG1 should only be changed while BRG1 is disabled to prevent spurious counts.

Bit combination 00 selects the output of CTR0 as the clock source for BRG1. It is advisable to enable CTR0 and select its clock source in a separate write to this register.

Bit combination 01 selects the output of CTR1 as the clock source for BRG1. It is advisable to enable CTR0 and select its clock source in a separate write to this register.

Bit combination 10 selects the /RxC pin as the clock source for BRG1.

Bit combination 11 selects the /TxC pin as the clock source for BRG1.

5.11.4 BRG0 Clock Source Control Field

Bits 9 and 8 are used to select the source of the clock for BRG0. The clock source for BRG0 should only be changed while BRG0 is disabled to prevent spurious counts.

Bit combination 00 selects the output of CTR0 as the clock source for BRG0. It is advisable to enable CTR0 and select its clock source in a separate write to this register.

Bit combination 01 selects the output of CTR1 as the clock source for BRG0. It is advisable to enable CTR0 and select its clock source in a separate write to this register.

Bit combination 10 selects the /RxC pin as the clock source for BRG0.

Bit combination 11 selects the /TxC pin as the clock source for BRG0.

5.11.5 DPLL Clock Source Control Field

Bits 7 and 6 are used to select the source of the clock for the DPLL. The clock source for the DPLL should only be changed while DPLL is disabled to prevent spurious sequences in the DPLL state machine.

Bit combination 00 selects the output of BRG0 as the clock source for the DPLL.

Bit combination 01 selects the output of BRG1 as the clock source for the DPLL.

Bit combination 10 selects the /RxC pin as the clock source for the DPLL.

Bit combination 11 selects the /TxC pin as the clock source for the DPLL.

5.11.6 Transmit Clock Source Control Field

Bits 5 through 3 are used to select the source of the clock for the transmitter. The clock source for the transmitter should only be changed while the transmitter is disabled to prevent spurious sequences in the transmit state machine.

Bit combination 000 disables the clock to the transmitter and forces the transmit clock Low. During channel reset, the clock is pulsed High to reset all of the flip-flops and latches in the transmitter.

Bit combination 001 selects the /RxC pin as the clock source for the transmitter.

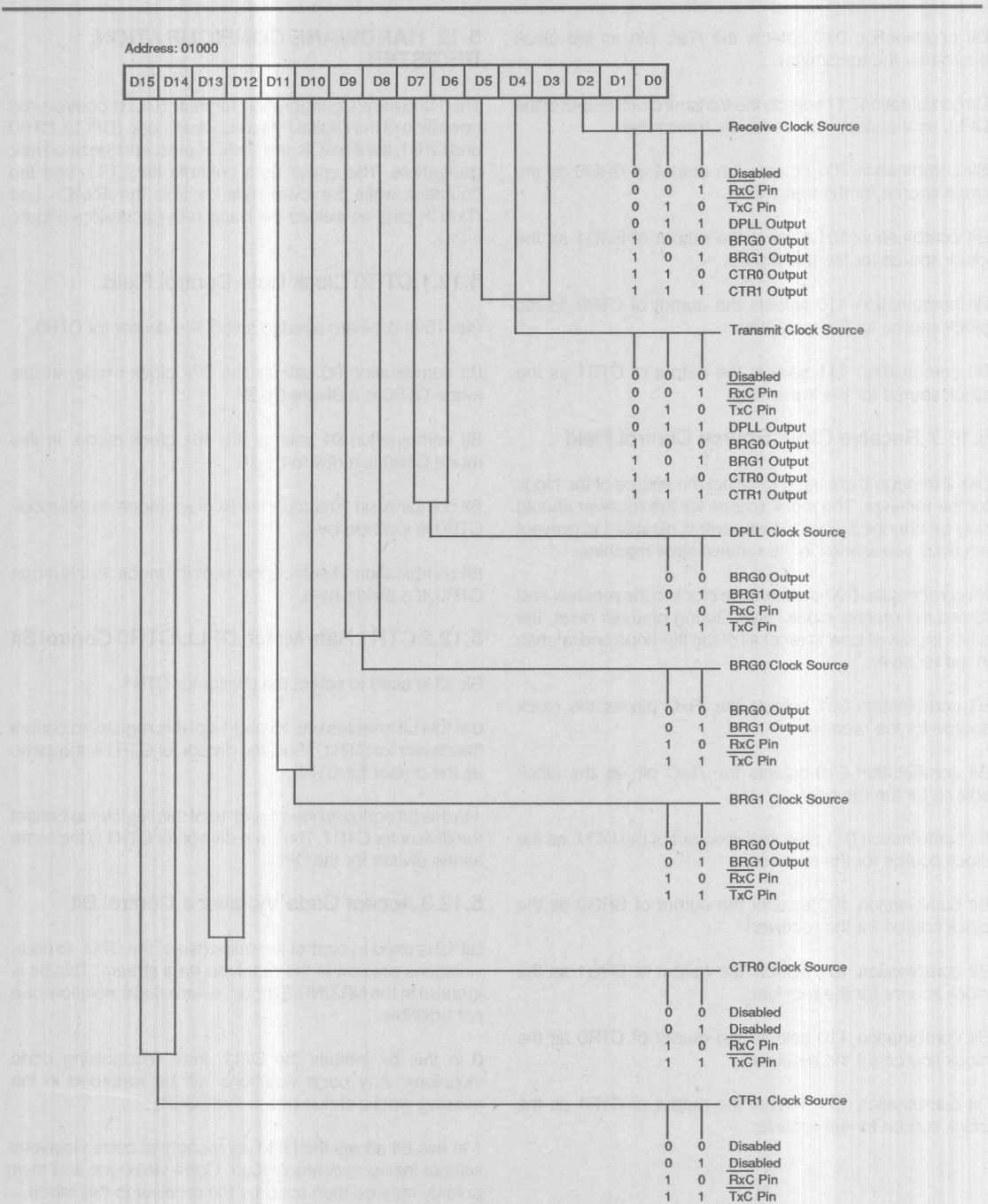


Figure 5-23. Clock Mode Control Register

Bit combination 010 selects the /TxC pin as the clock source for the transmitter.

Bit combination 011 selects the transmit clock output of the DPLL as the clock source for the transmitter.

Bit combination 100 selects the output of BRG0 as the clock source for the transmitter.

Bit combination 101 selects the output of BRG1 as the clock source for the transmitter.

Bit combination 110 selects the output of CTR0 as the clock source for the transmitter.

Bit combination 111 selects the output of CTR1 as the clock source for the transmitter.

5.11.7 Receive Clock Source Control Field

Bits 2 through 0 are used to select the source of the clock for the receiver. The clock source for the receiver should only be changed while the receiver is disabled to prevent spurious sequences in the receive state machine.

Bit combination 000 disables the clock to the receiver and forces the receive clock High. During channel reset, the clock is pulsed Low to reset all of the flip-flops and latches in the receiver.

Bit combination 001 selects the /RxC pin as the clock source for the receiver.

Bit combination 010 selects the /TxC pin as the clock source for the receiver.

Bit combination 011 selects the output of the DPLL as the clock source for the receiver.

Bit combination 100 selects the output of BRG0 as the clock source for the receiver.

Bit combination 101 selects the output of BRG1 as the clock source for the receiver.

Bit combination 110 selects the output of CTR0 as the clock source for the receiver.

Bit combination 111 selects the output of CTR1 as the clock source for the receiver.

5.12 HARDWARE CONFIGURATION REGISTER

The Hardware Configuration register (HCR) controls the operation of the Digital Phase-Locked Loop (DPLL), CTR0 and CTR1, the /RxACK and /TxACK pins, and the baud rate generators. The upper byte controls the DPLL and the counters, while the lower byte controls the /RxACK and /TxACK pins as well as the baud rate generators (Figure 5-24).

5.12.1 CTR0 Clock Rate Control Field

Bits 15 and 14 are used to select the divisor for CTR0.

Bit combination 00 selects the 32x clock mode. In this mode CTR0 is a divide-by-32.

Bit combination 01 selects the 16x clock mode. In this mode CTR0 is a divide-by-16.

Bit combination 10 selects the 8x clock mode. In this mode CTR0 is a divide-by-8.

Bit combination 11 selects the 4x clock mode. In this mode CTR0 is a divide-by-4.

5.12.2 CTR1 Rate Match DPLL/CTR0 Control Bit

Bit 13 is used to select the divisor for CTR1.

0 in this bit enables bits 15 and 14 of this register to control the divisor for CTR1. Thus, the divisor for CTR1 is the same as the divisor for CTR0.

1 in this bit enables bits 11 and 10 of this register to control the divisor for CTR1. Thus, the divisor for CTR1 is the same as the divisor for the DPLL.

5.12.3 Accept Code Violations Control Bit

Bit 12 is used to control the response of the DPLL to code violations present in the received data stream. This bit is ignored in the NRZ/NRZI mode, where code violations are not possible.

0 in this bit inhibits the DPLL from recognizing code violations. Any code violations will be recorded in the missing clocks status bits in the CCSR.

1 in this bit allows the DPLL to recognize code violations without losing synchronization. Code violations and their polarity may be then used by the receiver in this mode.

Address: 01001

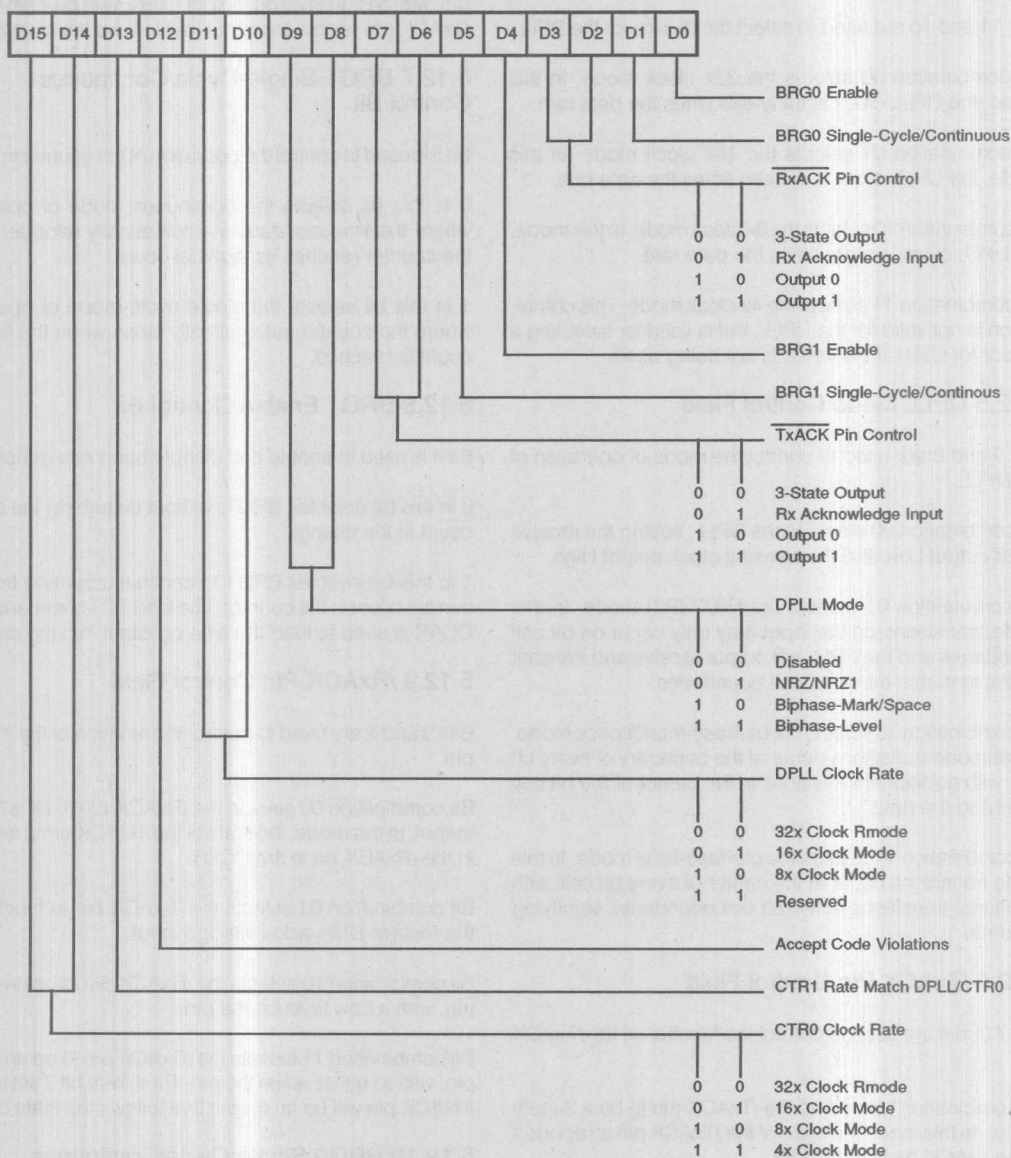


Figure 5-24. Hardware Configuration Register

5.12.4 DPLL Clock Rate Control Field

Bits 11 and 10 are used to select the divisor for the DPLL.

Bit combination 00 selects the 32x clock mode. In this mode, the DPLL clock is thirty-two times the data rate.

Bit combination 01 selects the 16x clock mode. In this mode, the DPLL clock is sixteen times the data rate.

Bit combination 10 selects the 8x clock mode. In this mode, the DPLL clock is eight times the data rate.

Bit combination 11 selects the 4x clock mode. This combination is not valid for the DPLL, but is valid for selecting a divisor for CTR1 if the DPLL is not being used.

5.12.5 DPLL Mode Control Field

Bits 9 and 8 are used to control the mode of operation of the DPLL.

Bit combination 00 disables the DPLL, setting the receive clock output Low and the transmit clock output High.

Bit combination 01 selects the NRZ/NRZI mode. In this mode, transitions on the input may only occur on bit cell boundaries and the DPLL will output receive and transmit clocks to match these bit cell boundaries.

Bit combination 10 selects the biphase-mark/space mode. In this mode transitions occur at the boundary of every bit cell, with additional transitions in the center of the bit cell signifying the data.

Bit combination 11 selects the biphase-level mode. In this mode transitions occur at the center of every bit cell, with additional transitions at the bit cell boundaries signifying the data.

5.12.6 /TxACK Pin Control Field

Bits 7 and 6 are used to control the function of the /TxACK pin.

Bit combination 00 selects the /TxACK pin to be a 3-state output. In this mode the state of the /TxACK pin is reported in the TxACK bit in the CCSR.

Bit combination 01 selects the /TxACK pin to function as the transmit DMA acknowledge input.

Bit combination 10 selects the /TxACK pin to be an output pin, with a Low level on the pin.

Bit combination 11 selects the /TxACK pin to be an output pin, with a High level on the pin. Thus, with bit 7 set to 1 the /TxACK pin will be an output that follows the state of bit 6.

5.12.7 BRG1 Single-Cycle/Continuous Control Bit

Bit 5 is used to control the operation of the counter in BRG1.

0 in this bit selects the continuous mode of operation, where the time constant is automatically reloaded when the counter reaches its terminal count.

1 in this bit selects the single-cycle mode of operation, where the counter automatically stops when the terminal count is reached.

5.12.8 BRG1 Enable Control Bit

Bit 4 is used to enable and disable baud rate generator 1.

0 in this bit disables BRG1, without disturbing the current count in the counter.

1 in this bit enables BRG1 to continue counting from the current count in the counter. The load TC1 command in the CCAR is used to load the time constant into the counter.

5.12.9 /RxACK Pin Control Field

Bits 3 and 2 are used to control the function of the /RxACK pin.

Bit combination 00 selects the /RxACK pin to be a 3-state output. In this mode, the state of the /RxACK pin is reported in the /RxACK bit in the CCSR.

Bit combination 01 selects the /RxACK pin to function as the receive DMA acknowledge input.

Bit combination 10 selects the /RxACK pin to be an output pin, with a Low level on the pin.

Bit combination 11 selects the /RxACK pin to be an output pin, with a High level on the pin. Thus, with bit 3 set to 1 the /RxACK pin will be an output that follows the state of bit 2.

5.12.10 BRG0 Single Cycle/Continuous Control Bit

Bit 1 is used to control the operation of the counter in BRG0.

0 in this bit selects the continuous mode of operation, where the time constant is automatically reloaded when the counter reaches its terminal count.

1 in this bit selects the single-cycle mode of operation, where the counter automatically stops when the terminal count is reached.

5.12.11 BRG0 Enable Control Bit

Bit 0 is used to enable and disable baud rate generator 0.

0 in this bit disables BRG0, without disturbing the current count in the counter.

1 in this bit enables BRG0 to continue counting from the current count in the counter. The load TCO command in the CCAR is used to load the time constant into the counter.

5.13 INTERRUPT VECTOR REGISTER

The Interrupt Vector Register (IVR) contains the interrupt vector, that is returned by the device during an interrupt acknowledge cycle. The lower byte of the register contains the vector written by the CPU, while the upper byte contains the vector modified by any interrupt conditions that may exist. The upper byte of this register always reflects the interrupt status, independent of the VIS bit or the VIS Level control field in the ICR. The interrupt vector returned by the device during an interrupt acknowledge, on the other hand, is always controlled by the VIS bit and the VIS Level control field in the ICR (Figure 5-25).

5.13.1 Interrupt Vector Status Field

Bits 15 through 12 and 8 are copies of bits 7 through 4 and 0 of the IVR, while bits 11 through 9 are encoded to indicate

the highest priority interrupt pending in the channel as shown below:

Bit combination 000 indicates that there are no interrupts pending in the channel.

Bit combination 001 indicates that a device status interrupt is the highest priority interrupt pending in the channel.

Bit combination 010 indicates that an I/O status interrupt is the highest priority interrupt pending in the channel.

Bit combination 011 indicates that a transmit data interrupt is the highest priority interrupt pending in the channel.

Bit combination 100 indicates that a transmit status interrupt is the highest priority interrupt pending in the channel.

Bit combination 101 indicates that a receive data interrupt is the highest priority interrupt pending in the channel.

Bit combination 110 indicates that a receive status interrupt is the highest priority interrupt pending in the channel.

Bit combination 111 is not used and will never be returned by the channel.

5.13.2 Interrupt Vector Control Field

Bits 7 through 0 contain the interrupt vector as written by the CPU. Any bit combination is allowed.

Address: 01010

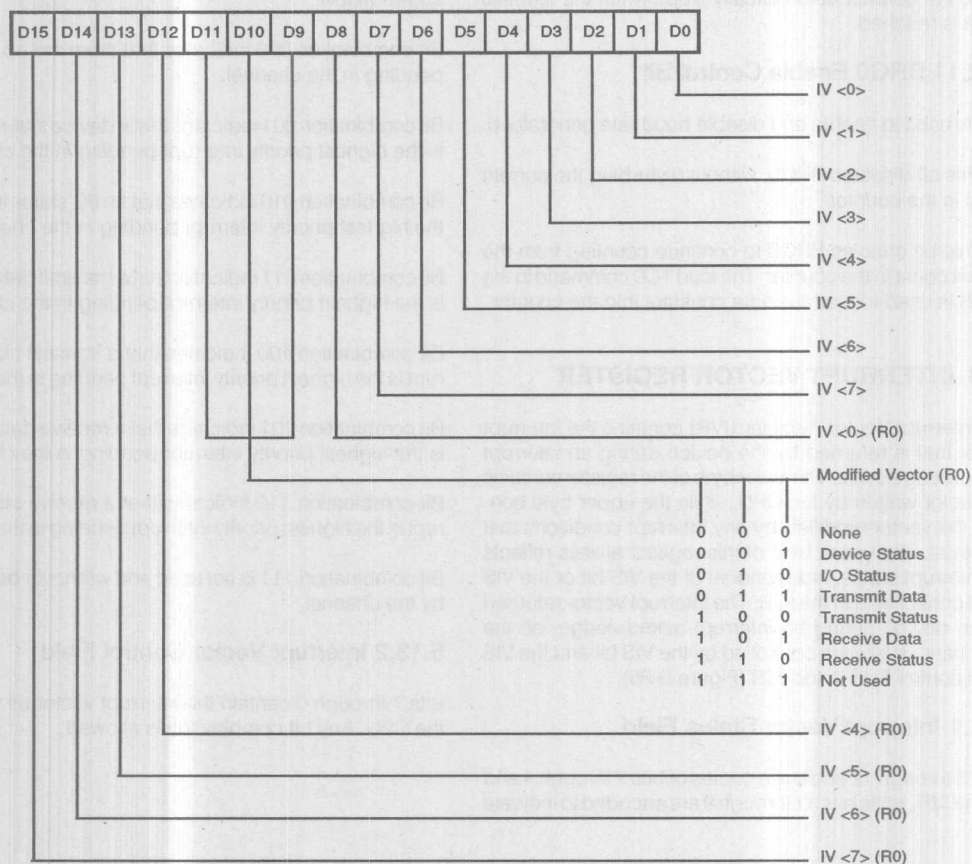


Figure 5-25. Interrupt Vector Register

5.14 I/O CONTROL REGISTER

The I/O Control Register (IOCR) contains control fields to select the modes for the various pins in the channel (Figure 5-26).

5.14.1 /CTS Pin Control Field

Bits 15 and 14 are used to control the function of the /CTS pin.

Bit combination 00 selects the /CTS pin to function as a /CTS input.

Bit combination 01 selects the /CTS pin to function as a /CTS input.

Bit combination 10 selects the /CTS pin to be an output pin, with a Low level on the pin.

Bit combination 11 selects the /CTS pin to be an output pin, with a High level on the pin. Thus, with bit 15 set to 1 the /CTS output pin will follow the state of bit 14.

Address: 01011

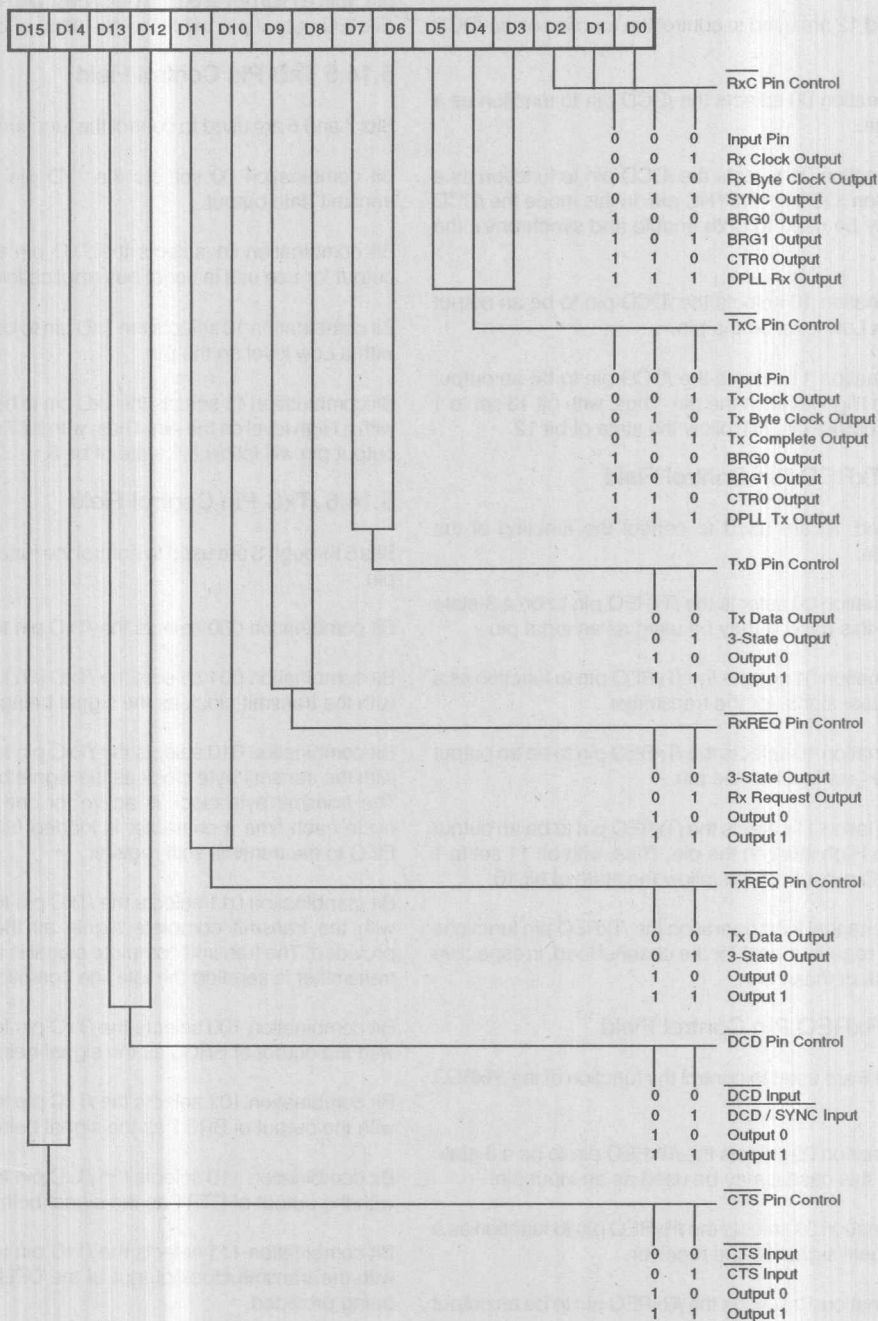


Figure 5-26 I/O Control Register

5.14.2 /DCD Pin Control Field

Bits 13 and 12 are used to control the function of the /DCD pin.

Bit combination 00 selects the /DCD pin to function as a /DCD input.

Bit combination 01 selects the /DCD pin to function as a combination /DCD and /SYNC pin. In this mode the /DCD signal may be used to both enable and synchronize the receiver.

Bit combination 10 selects the /DCD pin to be an output pin, with a Low level on the pin.

Bit combination 11 selects the /DCD pin to be an output pin, with a High level on the pin. Thus, with bit 13 set to 1 the /DCD output pin will follow the state of bit 12.

5.14.3 /TxREQ Pin Control Field

Bits 11 and 10 are used to control the function of the /TxREQ pin.

Bit combination 00 selects the /TxREQ pin to be a 3-state output. In this case, it may be used as an input pin.

Bit combination 01 selects the /TxREQ pin to function as a DMA request signal for the transmitter.

Bit combination 10 selects the /TxREQ pin to be an output pin, with a Low level on the pin.

Bit combination 11 selects the /TxREQ pin to be an output pin, with a High level on the pin. Thus, with bit 11 set to 1 the /TxREQ output pin will follow the state of bit 10.

During a channel load operation the /TxREQ pin functions as a DMA request signal for the channel load, irrespective of the state of these bits.

5.14.4 /RxREQ Pin Control Field

Bits 9 and 8 are used to control the function of the /RxREQ pin.

Bit combination 00 selects the /RxREQ pin to be a 3-state output. In this case it may be used as an input pin.

Bit combination 01 selects the /RxREQ pin to function as a DMA request signal for the receiver.

Bit combination 10 selects the /RxREQ pin to be an output pin, with a Low level on the pin.

Bit combination 11 selects the /RxREQ pin to be an output pin, with a High level on the pin. Thus, with bit 9 set to 1 the /RxREQ output pin will follow the state of bit 8.

5.14.5 TxD Pin Control Field

Bits 7 and 6 are used to control the function of the TxD pin.

Bit combination 00 selects the TxD pin to provide the transmit data output.

Bit combination 01 selects the TxD pin to be a 3-state output for use in serial bus applications.

Bit combination 10 selects the TxD pin to be an output pin, with a Low level on the pin.

Bit combination 11 selects the TxD pin to be an output pin, with a High level on the pin. Thus, with bit 7 set to 1 the TxD output pin will follow the state of bit 6.

5.14.6 /TxC Pin Control Field

Bits 5 through 3 are used to control the function of the /TxC pin.

Bit combination 000 selects the /TxC pin to be an input.

Bit combination 001 selects the /TxC pin to be an output, with the transmit clock as the signal being provided.

Bit combination 010 selects the /TxC pin to be an output, with the transmit byte clock as the signal being provided. The transmit byte clock is active for one transmit clock cycle each time a character is loaded from the transmit FIFO to the transmit shift register.

Bit combination 011 selects the /TxC pin to be an output, with the transmit complete signal as the signal being provided. The transmit complete signal is active while the transmitter is sending the idle line condition.

Bit combination 100 selects the /TxC pin to be an output, with the output of BRG0 as the signal being provided.

Bit combination 101 selects the /TxC pin to be an output, with the output of BRG1 as the signal being provided.

Bit combination 110 selects the /TxC pin to be an output, with the output of CTR1 as the signal being provided.

Bit combination 111 selects the /TxC pin to be an output, with the transmit clock output of the DPLL as the signal being provided.

5.14.7 /RxC Pin Control Field

Bits 2 through 0 are used to control the function of the /RxC pin.

Bit combination 000 selects the /RxC pin to be an input.

Bit combination 001 selects the /RxC pin to be an output, with the receive clock as the signal being provided.

Bit combination 010 selects the /RxC pin to be an output, with the receive byte clock as the signal being provided. The receive byte clock is active for one receive clock cycle each time a character is loaded from the receive shift register to the receive FIFO.

Bit combination 011 selects the /RxC pin to be an output, with the receive sync signal as the signal being provided. The receive sync signal is active for one receive clock cycle upon receipt of a sync character or flag, as appropriate for the receive mode.

Bit combination 100 selects the /RxC pin to be an output, with the output of BRG0 as the signal being provided.

Bit combination 101 selects the /RxC pin to be an output, with the output of BRG1 as the signal being provided.

Bit combination 110 selects the /RxC pin to be an output, with the output of CTR0 as the signal being provided.

Bit combination 111 selects the /RxC pin to be an output, with the receive clock output of the DPLL as the signal being provided.

5.15 INTERRUPT CONTROL REGISTER

The Interrupt Control Register (ICR) contains the control bits for the interrupts in the channel. The upper byte of the ICR controls the daisy-chain, while the lower byte controls the Interrupt Enable (IE) bits for the different sources of interrupt (Figure 5-27).

5.15.1 Master Interrupt Enable Control Bit

Bit 15 is the global control bit for the channel interrupts.

0 in this bit disables all interrupts for the channel, independent of the individual enables. While this bit is set to 0, the channel IEO will follow the state of the channel IEI unless there is an IUS set in the channel or the DLC bit is set to 1.

1 in this bit enables the interrupt logic to operate normally.

5.15.2 Disable Lower Chain Control Bit

Bit 14 is used to control any lower priority external interrupt daisy-chain.

0 in this bit enables the interrupt daisy-chain below the channel to operate normally.

1 in this bit disables all interrupts having lower priority than the channel, by forcing the IEO output of the channel to be 0. The daisy-chain within the channel continues to operate normally.

5.15.3 No Vector Control Bit

Bit 13 is used to control the response of the channel to an interrupt acknowledge cycle.

0 in this bit enables the channel to provide an interrupt vector during an interrupt acknowledge cycle. The vector returned during an interrupt acknowledge cycle is the same width as the bus selected for the device. In the 16-bit case the low byte is either modified or unmodified, depending on the state of the VIS bit in this register. The high byte is always the modified vector.

1 in this bit disables the data bus drivers during an interrupt acknowledge cycle. Thus, no vector will be returned by the channel during an interrupt acknowledge cycle.

5.15.4 Vector Includes Status Control Bit

Bit 12 is used to control the encoding of status information in the vector that is returned during an interrupt acknowledge cycle.

0 in this bit, prevents the channel from modifying the vector to include status information during an interrupt acknowledge cycle; it is returned exactly as written in the IVR.

1 in this bit enables the channel to include status information in the vector returned during an interrupt acknowledge cycle.

5.15.5 Vector Includes Status Level Control Field

Bits 11 through 9 are used to control the status encoded in the vector returned during an interrupt acknowledge cycle. This vector is only modified if the source of interrupt is enabled to do so; otherwise it is returned exactly as written to the IVR. Both the high byte of the IVR and the high byte of the vector returned during an interrupt acknowledge cycle in the 16-bit bus case are always modified by the interrupt status.

Address: 01100

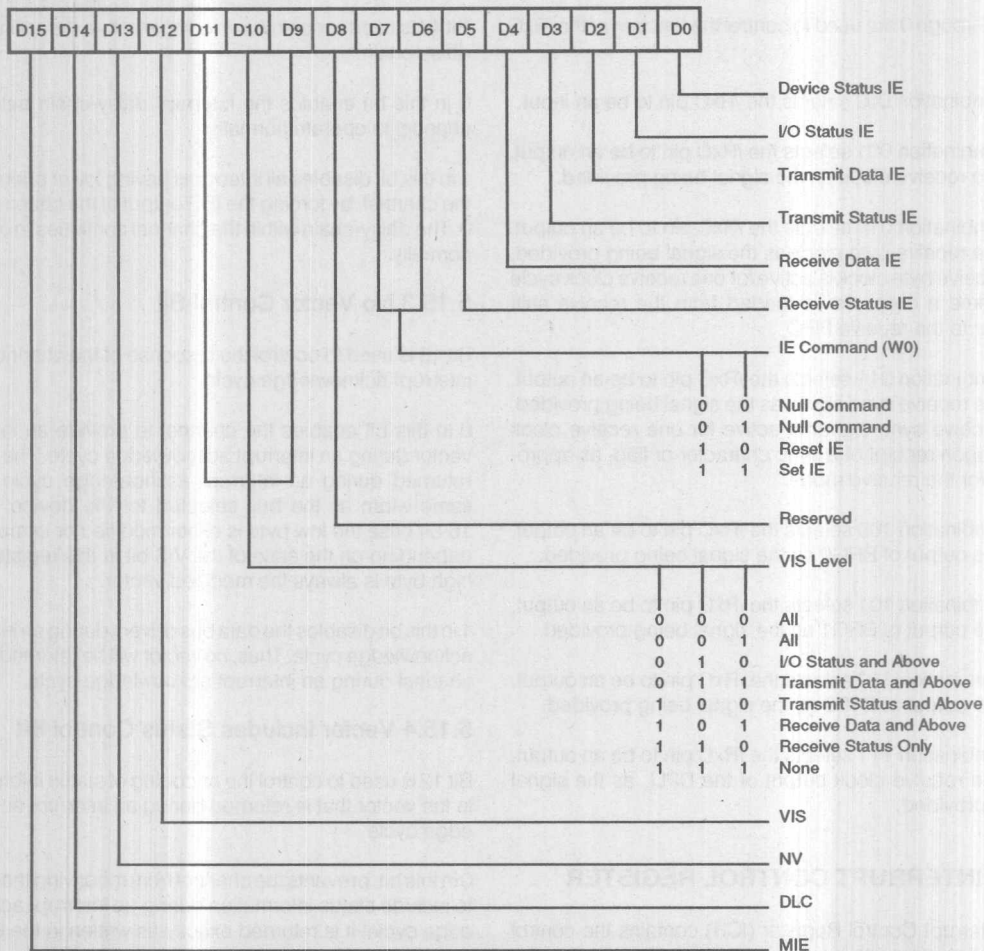


Figure 5-27. Interrupt Control Register

Bit combination 000 enables all sources of interrupt in the channel to modify the vector returned during an interrupt acknowledge cycle.

Bit combination 001 enables all sources of interrupt in the channel to modify the vector returned during an interrupt acknowledge cycle.

Bit combination 010 enables receive status, receive data, transmit status, transmit data and I/O status interrupts to

modify the vector returned during an interrupt acknowledge cycle. The channel will return an unmodified vector for a device status interrupt.

Bit combination 011 enables receive status, receive data, transmit status and transmit data interrupts to modify the vector returned during an interrupt acknowledge cycle. The channel will return an unmodified vector for I/O status and device status interrupts.

Bit combination 100 enables receive status, receive data and transmit status interrupts to modify the vector returned during an interrupt acknowledge cycle. The channel will return an unmodified vector for transmit data, I/O status and device status interrupts.

Bit combination 101 enables receive status and receive data interrupts to modify the vector returned during an interrupt acknowledge cycle. The channel will return an unmodified vector for transmit status, transmit data, I/O status and device status interrupts.

Bit combination 110 enables receive status interrupts to modify the vector returned during an interrupt acknowledge cycle. The channel will return an unmodified vector for receive data, transmit status, transmit data, I/O status and device status interrupts.

Bit combination 111 prevents the channel from modifying the vector to include status information during an interrupt acknowledge cycle.

5.15.6 Reserved Bit

Bit 8 is reserved and should not be used.

5.15.7 Interrupt Enable Command Field

Bits 7 and 6 are encoded with the commands for the interrupt enable bits for the six sources of interrupt as shown below:

Bit combination 00 is a null command and has no effect on the IE bits.

Bit combination 01 is a null command and has no effect on the IE bits.

Bit combination 10 is the reset IE command. Bits 5 through 0 of this register select those IE bits to be affected by this command.

Bit combination 11 is the set IE command. Bits 5 through 0 of this register select those IE bits to be affected by this command.

5.15.8 Receive Status Interrupt Enable Command/Status Bit

Bit 5 is the interrupt enable (IE) bit for receive status interrupts.

The Receive Status IE bit is written in conjunction with the IE command field in this register. If this command bit is 0

during a write operation to this register, the Receive Status IE bit is unaffected. If this command bit is 1 during a write operation to this register, the accompanying interrupt enable command will affect the Receive Status IE bit.

If the Receive Status IE bit is set to 0, receive status interrupts are disabled. The Receive Status IP bit will still be set when the interrupt condition occurs, but no interrupt request will be generated.

If the Receive Status IE bit is set to 1 receive status interrupts are enabled.

5.15.9 Receive Data Interrupt Enable Command/Status Bit

Bit 4 is the interrupt enable (IE) bit for receive data interrupts.

The Receive Data IE bit is written in conjunction with the IE command field in this register. If this command bit is 0 during a write operation to this register, the Receive Data IE bit is unaffected. If this command bit is 1 during a write operation to this register, the accompanying interrupt enable command will affect the Receive Data IE bit.

If the Receive Data IE bit is set to 0, receive data interrupts are disabled. The Receive Data IP bit will still be set when the interrupt condition occurs, but no interrupt request will be generated.

If the Receive Data IE bit is set to 1, receive data interrupts are enabled.

5.15.10 Transmit Status Interrupt Enable Command/Status Bit

Bit 3 is the interrupt enable (IE) bit for transmit status interrupts.

The Transmit Status IE bit is written in conjunction with the IE command field in this register. If this command bit is 0 during a write operation to this register, the Transmit Status IE bit is unaffected. If this command bit is 1 during a write operation to this register, the accompanying interrupt enable command will affect the Transmit Status IE bit.

If the Transmit Status IE bit is set to 0, transmit status interrupts are disabled. The Transmit Status IP bit will still be set when the interrupt condition occurs, but no interrupt request will be generated.

If the Transmit Status IE bit is set to 1, transmit status interrupts are enabled.

5.15.11 Transmit Data Interrupt Enable Command/Status Bit

Bit 2 is the interrupt enable (IE) bit for transmit data interrupts.

The Transmit Data IE bit is written in conjunction with the IE command field in this register. If this command bit is 0 during a write operation to this register, the Transmit Data IE bit is unaffected. If this command bit is 1 during a write operation to this register, the accompanying interrupt enable command will affect the Transmit Data IE bit.

If the Transmit Data IE bit is set to 0, transmit data interrupts are disabled. The Transmit Data IP bit will still be set when the interrupt condition occurs, but no interrupt request will be generated.

If the Transmit Data IE bit is set to 1, transmit data interrupts are enabled.

5.15.12 I/O Status Interrupt Enable Command/Status Bit

Bit 1 is the interrupt enable (IE) bit for I/O status interrupts.

The I/O Status IE bit is written in conjunction with the IE command field in this register. If this command bit is 0 during a write operation to this register, the I/O Status IE bit is unaffected. If this command bit is 1 during a write operation to this register, the accompanying interrupt enable command will affect the I/O Status IE bit.

If the I/O Status IE bit is set to 0, I/O status interrupts are disabled. The I/O Status IP bit will still be set when the interrupt condition occurs, but no interrupt request will be generated.

If the I/O Status IE bit is set to 1, I/O status interrupts are enabled.

5.15.13 Device Status Interrupt Enable Command/Status Bit

Bit 0 is the interrupt enable (IE) bit for device status interrupts.

The Device Status IE bit is written in conjunction with the IE command field in this register. If this command bit is 0 during a write operation to this register, the Device Status IE bit is unaffected. If this command bit is 1 during a write operation to this register, the accompanying interrupt enable command will affect the Device Status IE bit.

If the Device Status IE bit is set to 0, device status interrupts are disabled. The Device Status IP bit will still be set when

the interrupt condition occurs, but no interrupt request will be generated.

If the Device Status IE bit is set to 1, device status interrupts are enabled.

5.16 DAISY-CHAIN CONTROL REGISTER

The Daisy-Chain Control Register (DCCR) controls the Interrupt Pending (IP) and Interrupt-Under-Service (IUS) bits. The IP bits reside in the lower byte, while the IUS bits reside in the upper byte (Figure 5-28).

5.16.1 IUS Command Field

Bits 15 and 14 are encoded with the commands for the IUS bits for the six sources of interrupt as shown below:

Bit combination 00 is a null command and has no effect on the IUS bits.

Bit combination 01 is a null command and has no effect on the IUS bits.

Bit combination 10 is the reset IUS command. Bits 13 through 8 of the register select those IUS bits to be affected by this command.

Bit combination 11 is the set IUS command. Bits 13 through 8 of the register select those IUS bits to be affected by this command.

5.16.2 Receive Status IUS Command/Status Bit

Bit 13 is the IUS bit for receive status interrupts.

This bit may be written in conjunction with the IUS command field in this register. If this bit is set to 0 during a write operation to this register the Receive Status IUS bit is unaffected. If this bit is set to 1 during a write operation to this register the accompanying IUS command will affect the Receive Status IUS bit.

The Receive Status IUS bit will be set to 1 automatically during an interrupt acknowledge cycle if this is the highest priority interrupt pending. This is the highest priority interrupt pending if the IEI for this interrupt source is 1 and the corresponding IP is set to 1.

If the Receive Status IUS bit is set to 1, the receive status interrupt has been acknowledged and is under service. All lower priority interrupts are disabled (via the internal daisy-chain) and another receive status interrupt may not be requested.

Address: 01101

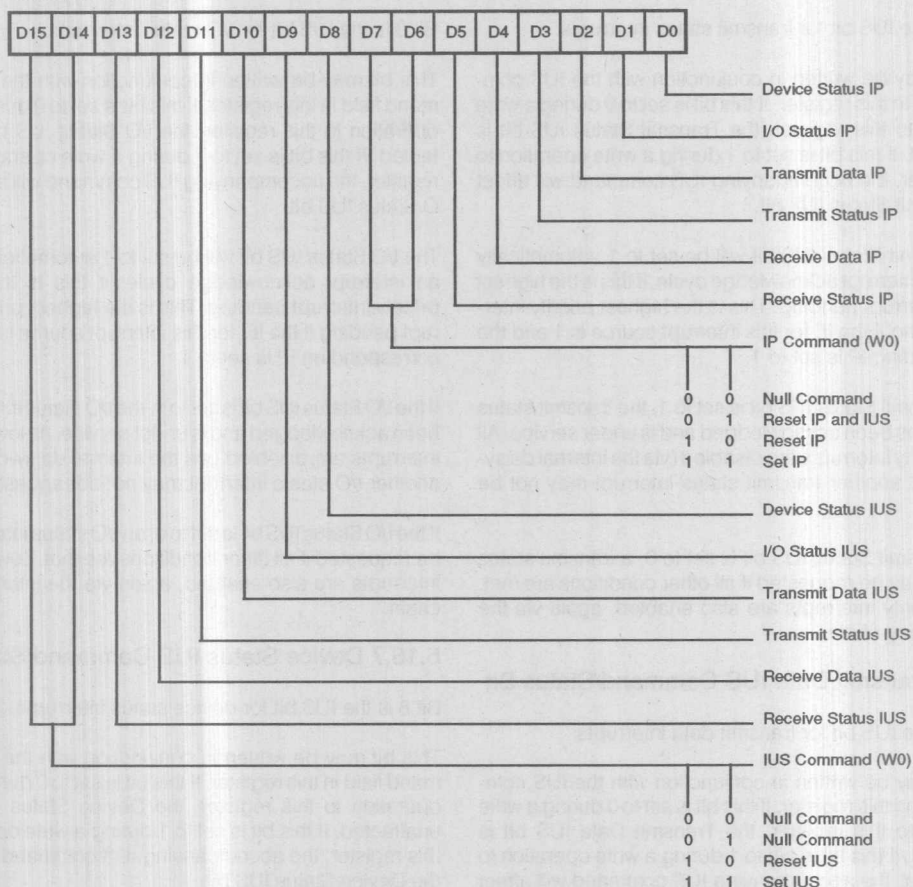


Figure 5-28. Daisy-Chain Control Register

If the Receive Status IUS bit is set to 0, a receive status interrupt may be requested if all other conditions are met. Lower priority interrupts are also enabled, again via the internal daisy chain.

5.16.3 Receive Data IUS Command/Status Bit

Bit 12 is the IUS bit for receive data interrupts.

This bit may be written in conjunction with the IUS command field in this register. If this bit is set to 0 during a write operation to this register, the Receive Data IUS bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IUS command will affect the Receive Data IUS bit.

The Receive Data IUS bit will be set to 1 automatically during an interrupt acknowledge cycle if this is the highest priority interrupt pending. This is the highest priority interrupt pending if the IEI for this interrupt source is 1 and the corresponding IP is set to 1.

If the Receive Data IUS bit is set to 1, the receive status interrupt has been acknowledged and is under service. All lower priority interrupts are disabled (via the internal daisy-chain) and another receive data interrupt may not be requested.

If the Receive Data IUS bit is set to 0, a receive data interrupt may be requested if all other conditions are met. Lower priority interrupts are also enabled, again via the internal daisy chain.

5.16.4 Transmit Status IUS Command/Status Bit

Bit 11 is the IUS bit for transmit status interrupts.

This bit may be written in conjunction with the IUS command field in this register. If this bit is set to 0 during a write operation to this register, the Transmit Status IUS bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IUS command will affect the Transmit Status IUS bit.

The Transmit Status IUS bit will be set to 1 automatically during an interrupt acknowledge cycle, if this is the highest priority interrupt pending. This is the highest priority interrupt pending if the IE for this interrupt source is 1 and the corresponding IP is set to 1.

If the Transmit Status IUS bit is set to 1, the transmit status interrupt has been acknowledged and is under service. All lower priority interrupts are disabled (via the internal daisy-chain) and another transmit status interrupt may not be requested.

If the Transmit Status IUS bit is set to 0, a transmit status interrupt may be requested if all other conditions are met. Lower priority interrupts are also enabled, again via the internal daisy-chain.

5.16.5 Transmit Data IUS Command/Status Bit

Bit 10 is the IUS bit for transmit data interrupts.

This bit may be written in conjunction with the IUS command field in this register. If this bit is set to 0 during a write operation to this register, the Transmit Data IUS bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IUS command will affect the Transmit Data IUS bit.

The Transmit Data IUS bit will be set to 1 automatically during an interrupt acknowledge cycle if this is the highest priority interrupt pending. This is the highest priority interrupt pending if the IEI for this interrupt source is 1 and the corresponding IP is set to 1.

If the Transmit Data IUS bit is set to 1, the transmit data interrupt has been acknowledged and is under service. All lower priority interrupts are disabled (via the internal daisy-chain) and another transmit data interrupt may not be requested.

If the Transmit Data IUS bit is set to 0, a transmit data interrupt may be requested if all other conditions are met. Lower priority interrupts are also enabled, again via the internal daisy-chain.

5.15.6 I/O Status IUS Command/Status Bit

Bit 9 is the IUS bit for I/O status interrupts.

This bit may be written in conjunction with the IUS command field in this register. If this bit is set to 0 during a write operation to this register, the I/O Status IUS bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IUS command will affect the I/O Status IUS bit.

The I/O Status IUS bit will be set to 1 automatically during an interrupt acknowledge cycle, if this is the highest priority interrupt pending. This is the highest priority interrupt pending if the IEI for this interrupt source is 1 and the corresponding IP is set to 1.

If the I/O Status IUS bit is set to 1, the I/O status interrupt has been acknowledged and is under service. All lower priority interrupts are disabled (via the internal daisy-chain) and another I/O status interrupt may not be requested.

If the I/O Status IUS bit is set to 0, an I/O status interrupt may be requested if all other conditions are met. Lower priority interrupts are also enabled, again via the internal daisy-chain.

5.16.7 Device Status IUS Command/Status Bit

Bit 8 is the IUS bit for device status interrupts.

This bit may be written in conjunction with the IUS command field in this register. If this bit is set to 0 during a write operation to this register, the Device Status IUS bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IUS command will affect the Device Status IUS bit.

The Device Status IUS bit will be set to 1 automatically during an interrupt acknowledge cycle, if this is the highest priority interrupt pending. This is the highest priority interrupt pending if the IEI for this interrupt source is 1 and the corresponding IP is set to 1.

If the Device Status IUS bit is set to 1, the receive status interrupt has been acknowledged and is under service. All lower priority interrupts are disabled (via the internal daisy-chain) and another device status interrupt may not be requested.

If the Device Status IUS bit is set to 0, a device status interrupt may be requested if all other conditions are met. Lower priority interrupts are also enabled, again via the internal daisy-chain.

5.16.8 IP Command Field

Bits 7 and 6 are encoded with the commands for the IP bits for the six sources of interrupt as shown below:

Bit combination 00 is a null command and has no effect on the IP bits.

Bit combination 01 is the reset IP and IUS command. Bits 5 through 0 of the register select those IP and IUS bits to be affected by this command. This command overrides any concurrent IUS command in bits 15 and 14 of this register.

Bit combination 10 is the reset IP command. Bits 5 through 0 of the register select those IP bits to be affected by this command.

Bit combination 11 is the set IP command. Bits 5 through 0 of the register select those IP bits to be affected by this command.

5.16.9 Receive Status IP Command/Status Bit

Bit 5 is the IP bit for receive status interrupts.

This bit may be written in conjunction with the IP command field in this register. If this bit is set to 0 during a write operation to this register, the receive status IP bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IP command will affect the receive status IP bit.

The Receive Status IP bit will be set to 1 automatically when a receive status interrupt condition occurs. An interrupt will be requested if the corresponding IE bit is 1 and IUS bit is 0, and the IEI for this interrupt source is 1.

5.16.10 Receive Data IP Command/Status Bit

Bit 4 is the IP bit for receive data interrupts.

This bit may be written in conjunction with the IP command field in this register. If this bit is set to 0 during a write operation to this register, the receive data IP bit is unaffected. If this bit is set to 1 during a write operation to this register the accompanying IP command will affect the receive status IP bit.

The Receive Data IP bit will be set to 1 automatically when a receive data interrupt condition occurs. An interrupt will be requested if the corresponding IE bit is 1 and IUS bit is 0, and the IEI for this interrupt source is 1.

5.16.11 Transmit Status IP Command/Status Bit

Bit 3 is the IP bit for transmit status interrupts.

This bit may be written in conjunction with the IP command field in this register. If this bit is set to 0 during a write operation to this register, the transmit status IP bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IP command will affect the transmit status IP bit.

The Transmit Status IP bit will be set to 1 automatically when a transmit status interrupt condition occurs. An interrupt will be requested if the corresponding IE bit is 1 and IUS bit is 0, and the IEI for this interrupt source is 1.

5.16.12 Transmit Data IP Command/Status Bit

Bit 2 is the IP bit for transmit data interrupts.

This bit may be written in conjunction with the IP command field in this register. If this bit is set to 0 during a write operation to this register, the transmit status IP bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IP command will affect the transmit data IP bit.

The Transmit Data IP bit will be set to 1 automatically when a transmit data interrupt condition occurs. An interrupt will be requested if the corresponding IE bit is 1 and IUS bit is 0, and the IEI for this interrupt source is 1.

5.16.13 I/O Status IP Command/Status Bit

Bit 1 is the IP bit for I/O status interrupts.

This bit may be written in conjunction with the IP command field in this register. If this bit is set to 0 during a write operation to this register, the I/O Status IP bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IP command will affect the transmit data IP bit.

The I/O Status IP bit will be set to 1 automatically when an I/O status interrupt condition occurs. An interrupt will be requested if the corresponding IE bit is 1 and IUS bit is 0, and the IEI for this interrupt source is 1.

5.16.14 Device Status IP Command/Status Bit

Bit 0 is the IP bit for device status interrupts.

This bit may be written in conjunction with the IP command field in this register. If this bit is set to 0 during a write operation to this register, the Device Status IP bit is unaffected. If this bit is set to 1 during a write operation to this register, the accompanying IP command will affect the transmit data IP bit.

The Device Status IP bit will be set to 1 automatically when a device status interrupt condition occurs. An interrupt will be requested if the corresponding IE bit is 1 and IUS bit is 0, and the IEI for this interrupt source is 1.

5.17 MISCELLANEOUS INTERRUPT STATUS REGISTER

The Miscellaneous Interrupt Status register (MISR) contains the command and status bits for the various sources of I/O status and device status interrupts (Figure 5-29).

Those pins which are not programmed to generate I/O status interrupts should be programmed initially to allow the capture of a transition, which will close the latches and place the status bits in stable states. This prevents transitions on the pins from appearing in the middle of a read of this register and potentially causing problems in a system environment.

5.17.1 RxC Latched/Unlatch Command/Status Bit

Bit 15 is used as a status bit to signal that a transition has occurred on /RxC and as a command bit to open the latches that capture this transition.

This bit is held at 0 if neither transition on the /RxC pin has been programmed to cause an I/O status interrupt or if an enabled transition on the /RxC pin has not been detected.

This bit is set to 1, and both this bit and the RxC status bit are latched when an enabled transition on the /RxC pin is detected, or immediately after the latch is opened if one or more enabled transitions occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit resets and opens this latch and opens the latch for the RxC status bit.

5.17.2 RxC Status Bit

Bit 14 is used to report the state of the /RxC pin.

This bit reflects the inverted state of the /RxC pin and is latched when an enabled transition on the /RxC pin is detected.

The latch is opened when a 1 is written to the RxC Latched/Unlatch command/status bit in this register.

5.17.3 TxC Latched/Unlatch Command/Status Bit

Bit 13 is used as a status bit to signal that a transition has occurred on /TxC and as a command bit to open the latches that capture this transition.

This bit is held at 0 if neither transition on the /TxC pin has been programmed to cause an I/O status interrupt or if an enabled transition on the /TxC pin has not been detected.

This bit is set to 1, and both this bit and the TxC status bit are latched, when an enabled transition on the /TxC pin is detected or immediately after the latch is opened if one or more enabled transitions occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit resets and opens this latch and opens the latch for the TxC status bit.

5.17.4 TxC Status Bit

Bit 12 is used to report the state of the /TxC pin.

This bit reflects the inverted state of the /TxC pin and is latched when an enabled transition on the /TxC pin is detected.

The latch is opened when a 1 is written to the TxC Latched/Unlatch command/status bit in this register.

5.17.5 RxREQ Latched/Unlatch Command/Status Bit

Bit 11 is used as a status bit to signal that a transition has occurred on /RxREQ and as a command bit to open the latches that capture this transition.

This bit is held at 0 if neither transition on the /RxREQ pin has been programmed to cause an I/O status interrupt or if an enabled transition on the /RxREQ pin has not been detected.

Address: 01110

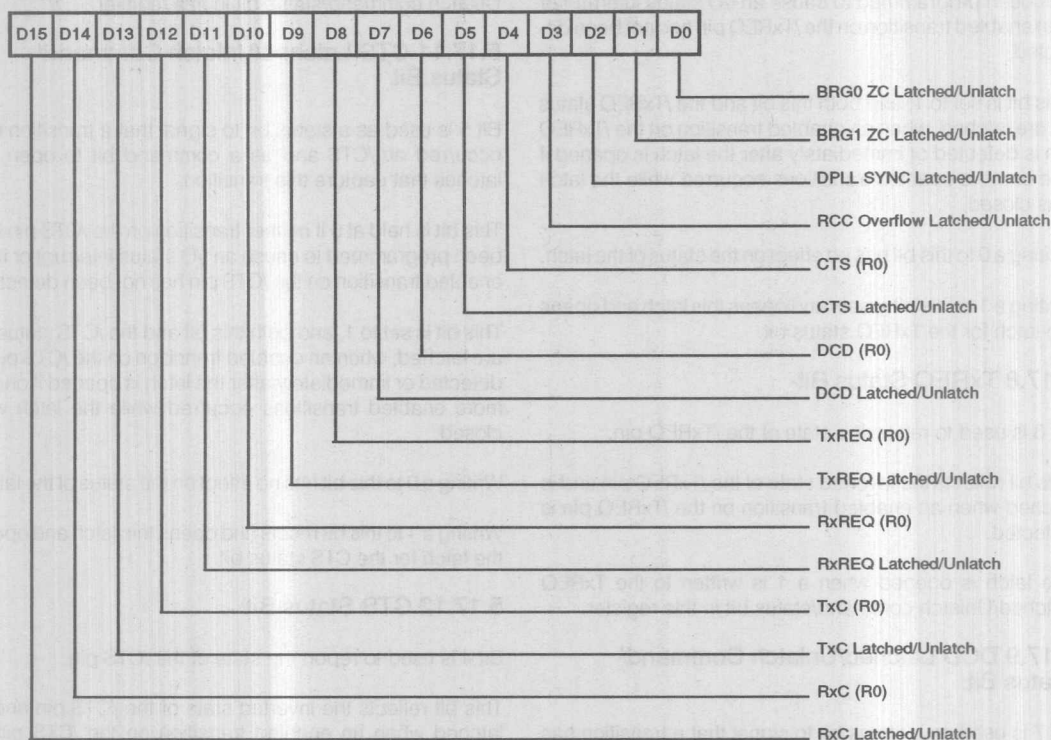


Figure 5-29. Miscellaneous Interrupt Status Register

This bit is set to 1, and both this bit and the RxREQ status bit are latched, when an enabled transition on the /RxREQ pin is detected or immediately after the latch is opened if one or more enabled transitions occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit resets and opens this latch and opens the latch for the RxREQ status bit.

5.17.6 RxREQ Status Bit

Bit 10 is used to report the state of the /RxREQ pin.

This bit reflects the inverted state of the /RxREQ pin and is latched when an enabled transition on the /RxREQ pin is detected.

The latch is opened when a 1 is written to the RxREQ Latched/Unlatch command/status bit in this register.

5.17.7 TxREQ Latched/Unlatch Command/Status Bit

Bit 9 is used as a status bit to signal that a transition has occurred on /TxREQ and as a command bit to open the latches that capture this transition.

This bit is held at 0 if neither transition on the /TxREQ pin has been programmed to cause an I/O status interrupt or if an enabled transition on the /TxREQ pin has not been detected.

This bit is set to 1, and both this bit and the /TxREQ status bit are latched, when an enabled transition on the /TxREQ pin is detected or immediately after the latch is opened if one or more enabled transitions occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit resets and opens this latch and opens the latch for the TxREQ status bit.

5.17.8 TxREQ Status Bit

Bit 8 is used to report the state of the /TxREQ pin.

This bit reflects the inverted state of the /TxREQ pin and is latched when an enabled transition on the /TxREQ pin is detected.

The latch is opened when a 1 is written to the TxREQ Latched/Unlatch command/status bit in this register.

5.17.9 DCD Latched/Unlatch Command/Status Bit

Bit 7 is used as a status bit to signal that a transition has occurred on /DCD and as a command bit to open the latches that capture this transition.

This bit is held at 0 if neither transition on the /DCD pin has been programmed to cause an I/O status interrupt or if an enabled transition on the /DCD pin has not been detected.

This bit is set to 1, and both this bit and the /DCD status bit are latched, when an enabled transition on the /DCD pin is detected or immediately after the latch is opened if one or more enabled transitions occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit resets and opens this latch and opens the latch for the DCD status bit.

5.17.10 DCD Status Bit

Bit 6 is used to report the state of the /DCD pin.

This bit reflects the inverted state of the /DCD pin and is latched when an enabled transition on the /DCD pin is detected.

The latch is opened when a 1 is written to the DCD Latched/Unlatch command/status bit in this register.

5.17.11 CTS Latched/Unlatch Command/Status Bit

Bit 5 is used as a status bit to signal that a transition has occurred on /CTS and as a command bit to open the latches that capture this transition.

This bit is held at 0 if neither transition on the /CTS pin has been programmed to cause an I/O status interrupt or if an enabled transition on the /CTS pin has not been detected.

This bit is set to 1, and both this bit and the /CTS status bit are latched, when an enabled transition on the /CTS pin is detected or immediately after the latch is opened if one or more enabled transitions occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit resets and opens this latch and opens the latch for the CTS status bit.

5.17.12 CTS Status Bit

Bit 4 is used to report the state of the /CTS pin.

This bit reflects the inverted state of the /CTS pin and is latched when an enabled transition on the /CTS pin is detected.

The latch is opened when a 1 is written to the CTS Latched/Unlatch command/status bit in this register.

5.17.13 RCC Overflow Latched/Unlatch Command/Status Bit

Bit 3 is used as a status bit to signal that a receive character count overflow has occurred and as a command bit to open the latch that captures this event.

This bit is held at 0 if the RCC overflow device status interrupt is disabled or until a receive character count overflow is detected.

This bit is set to 1 and latched when a receive character count overflow is detected or immediately after the latch is opened if another receive character count overflow occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit clears this bit and opens the latch.

5.17.14 DPLL Sync Latched/Unlatch Command/Status Bit

Bit 2 is used as a status bit to signal that the DPLL has lost synchronization and as a command bit to open the latch that captures this event.

This bit is held at 0 if the DPLL sync device status interrupt is disabled or until DPLL synchronization is lost.

This bit is set to 1 and latched when DPLL synchronization is lost or immediately after the latch is opened if another DPLL loss of synchronization occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit clears this bit and opens the latch.

5.17.15 BRG1 ZC Latched/Unlatch Command/Status Bit

Bit 1 is used as a status bit to signal that the BRG1 has reached the count of zero and as a command bit to open the latch that captures this event.

This bit is held at 0 if the BRG1 ZC device status interrupt is disabled or until the zero count condition is reached in BRG1.

This bit is set to 1 and latched when the zero count condition is reached in BRG1 or immediately after the latch is opened if another zero count condition in BRG1 occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit clears this bit and opens the latch.

5.17.16 BRG0 ZC Latched/Unlatch Command/Status Bit

Bit 0 is used as a status bit to signal that the BRG0 has reached the count of zero and as a command bit to open the latch that captures this event.

This bit is held at 0 if the BRG0 ZC device status interrupt is disabled or until the zero count condition is reached in BRG0.

This bit is set to 1 and latched when the zero count condition is reached in BRG0 or immediately after the latch is opened if another zero count condition in BRG0 occurred while the latch was closed.

Writing a 0 to this bit has no effect on the status of the latch.

Writing a 1 to this bit clears this bit and opens the latch.

5.18 STATUS INTERRUPT CONTROL REGISTER

The Status Interrupt Control Register (SICR) contains the control bits and fields for the various sources of I/O status and device status interrupts (Figure 5-30).

5.18.1 RxC Interrupts Control Field

Bits 15 and 14 are used to select which edge or edges on /RxC will cause an I/O status interrupt to be generated.

Bit combination 00 disables transitions on /RxC from generating an I/O status interrupt.

Bit combination 01 enables only the falling edge on /RxC to generate an I/O status interrupt.

Bit combination 10 enables only the rising edge on /RxC to generate an I/O status interrupt.

Bit combination 11 enables both edges on /RxC to generate I/O status interrupts.

Changing the value of these bits does not, in itself, cause an I/O status interrupt to be generated.

5.18.2 TxC Interrupts Control Field

Bits 13 and 12 are used to select which edge or edges on /TxC will cause an I/O status interrupt to be generated.

Bit combination 00 disables transitions on /TxC from generating an I/O status interrupt.

Bit combination 01 enables only the falling edge on /TxC to generate an I/O status interrupt.

Bit combination 10 enables only the rising edge on /TxC to generate an I/O status interrupt.

Bit combination 11 enables both edges on /TxC to generate I/O status interrupts.

Changing the value of these bits does not, in itself, cause an I/O status interrupt to be generated.



5.18.3 RxREQ Interrupts Control Field

Bits 11 and 10 are used to select which edge or edges on /RxREQ will cause an I/O status interrupt to be generated.

Bit combination 00 disables transitions on /RxREQ from generating an I/O status interrupt.

Bit combination 01 enables only the falling edge on /RxREQ to generate an I/O status interrupt.

Bit combination 10 enables only the rising edge on /RxREQ to generate an I/O status interrupt.

Bit combination 11 enables both edges on /RxREQ to generate I/O status interrupts.

Changing the value of these bits does not, in itself, cause an I/O status interrupt to be generated.

5.18.4 TxREQ Interrupts Control Field

Bits 9 and 8 are used to select which edge or edges on /TxREQ will cause an I/O status interrupt to be generated.

Bit combination 00 disables transitions on /TxREQ from generating an I/O status interrupt.

Bit combination 01 enables only the falling edge on /TxREQ to generate an I/O status interrupt.

Bit combination 10 enables only the rising edge on /TxREQ to generate an I/O status interrupt.

Bit combination 11 enables both edges on /TxREQ to generate I/O status interrupts.

Changing the value of these bits does not, in itself, cause an I/O status interrupt to be generated.

5.18.5 DCD Interrupts Control Field

Bits 7 and 6 are used to select which edge or edges on /DCD will cause an I/O status interrupt to be generated.

Bit combination 00 disables transitions on /DCD from generating an I/O status interrupt.

Bit combination 01 enables only the falling edge on /DCD to generate an I/O status interrupt.

Bit combination 10 enables only the rising edge on /DCD to generate an I/O status interrupt.

Bit combination 11 enables both edges on /DCD to generate I/O status interrupts.

Changing the value of these bits does not, in itself, cause an I/O status interrupt to be generated.

5.18.6 CTS Interrupts Control Field

Bits 5 and 4 are used to select which edge or edges on /CTS will cause an I/O status interrupt to be generated.

Bit combination 00 disables transitions on /CTS from generating an I/O status interrupt.

Bit combination 01 enables only the falling edge on /CTS to generate an I/O status interrupt.

Bit combination 10 enables only the rising edge on /CTS to generate an I/O status interrupt.

Bit combination 11 enables both edges on /CTS to generate I/O status interrupts.

Changing the value of these bits does not, in itself, cause an I/O status interrupt to be generated.

5.18.7 RCC Overflow Interrupt Enable Control Bit

Bit 3 is used to control receive character count overflow device status interrupts.

0 in this bit inhibits the overflow condition in the receive character counter from causing a device status interrupt to be generated.

1 in this bit enables the overflow condition in the receive character counter to generate a device status interrupt.

5.18.8 DPLL Sync Interrupt Enable Control Bit

Bit 2 is used to control DPLL loss of synchronization device status interrupts.

0 in this bit inhibits the loss of synchronization in the DPLL from causing a device status interrupt to be generated.

1 in this bit enables the loss of synchronization in the DPLL to generate a device status interrupt.

5.18.9 BRG1 ZC Interrupt Enable Control Bit

Bit 1 is used to control BRG1 zero count device status interrupts.

0 in this bit inhibits the zero count condition in BRG1 from causing a device status interrupt to be generated.

1 in this bit enables the zero count condition in BRG1 to generate a device status interrupt.

5.18.10 BRG0 ZC Interrupt Enable Control Bit

Bit 0 is used to control BRG0 zero count device status interrupts.

0 in this bit inhibits the zero count condition in BRG0 from causing a device status interrupt to be generated.

1 in this bit enables the zero count condition in BRG0 to generate a device status interrupt.

5.19 RECEIVE DATA REGISTER

The Receive Data Register (RDR) contains the two bytes at the top of the receive FIFO (Figure 5-31).

The RDR is a read-only register. Data may be written to the bottom of the receive data FIFO with the appropriate test mode access. The RDR may be addressed by the address

latched with the /AS signal, indirectly by the pointer in the CCAR, directly via the D//C pin active High, or directly through the /RxACK signal.

Either bytes or words may be read from the RDR. In the case of a byte read, the lower byte of the register must be used and internal logic will properly extract the data from the FIFO. In the case of a word read the byte ordering from the FIFO must be initially specified by a command in the CCAR. In the case of straight memory data, which is the default case, the most significant byte of the RDR (bits 15-8) is the data that was received first, with the least significant byte (bits 7-0) being the data that was received second. In the case of swapped memory data the least significant byte of the RDR (bits 7-0) is the data that was received first, with the most significant byte (bits 15-8) being the data that was received second.

The data in the receive FIFO is always received least significant bit (bit 0) first, but the bit order may be programmably swapped at the output of the FIFO via a command in the CCAR. The default case is no swap (LSB first).

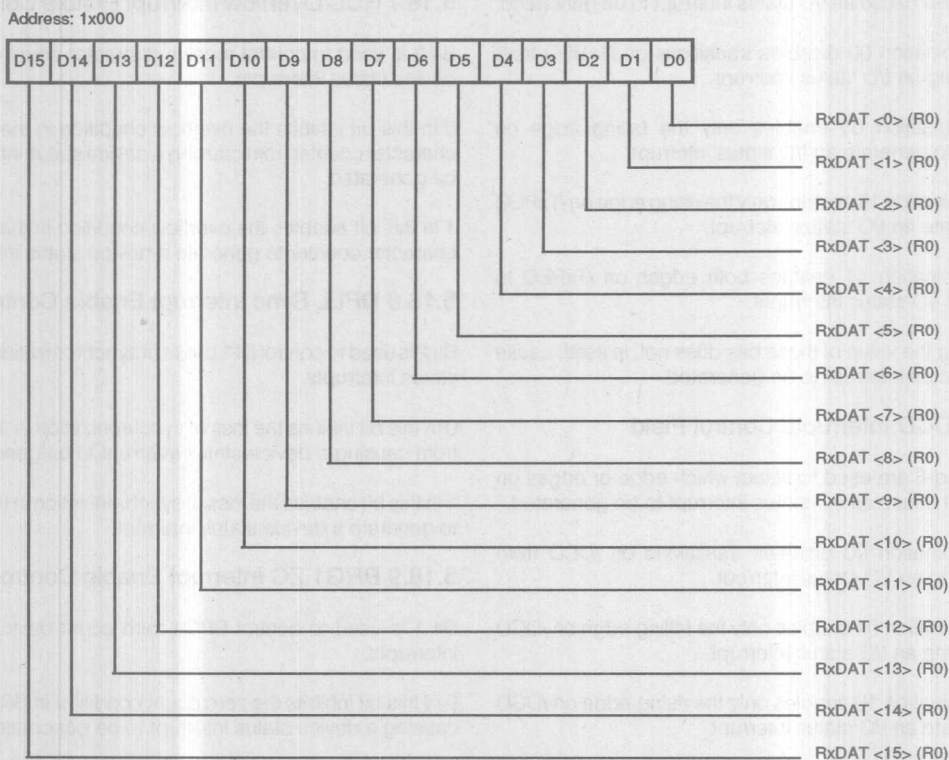


Figure 5-31. Receive Data Register

5.20 RECEIVE MODE REGISTER

The Receive Mode Register (RMR) contains various control bits for the receiver (Figure 5-32).

5.20.1 Receive Data Decoding Control Field

Bits 15 through 13 are used to select the data decoding method used by the receiver.

Bit combination 000 selects NRZ decoding. In NRZ a data bit of zero is represented by a logic 0 for the duration of the bit cell and a data bit of one is represented by a logic 1 for the duration of the bit cell.

Bit combination 001 selects NRZB decoding. In NRZB, a data bit of zero is represented by a logic 1 for the duration of the bit cell and a data bit of one is represented by a logic 0 for the duration of the bit cell.

Bit combination 010 selects NRZI-Mark decoding. In NRZI-Mark, a data bit of zero is represented by no transition at the beginning of the bit cell and a data bit of one is represented by a transition at the beginning of the bit cell. That is, the level present in the preceding bit cell is reversed for a one and continued for a zero.

Bit combination 011 selects NRZI-Space decoding. In NRZI-Space, a data bit of zero is represented by a transition at the beginning of the bit cell and a data bit of one is represented by no transition at the beginning of the bit cell. That is, the level present in the preceding bit cell is reversed for a zero and continued for a one.

Bit combination 100 selects Biphase-Mark decoding. In Biphase-Mark, a data bit of zero is represented by a transition at the beginning of the bit cell only and a data bit of one is represented by a transition at the beginning of the bit cell and another transition at the center of the bit cell. These transitions may be of either polarity.

Bit combination 101 selects Biphase-Space decoding. In Biphase-Space, a data bit of zero is represented by a transition at the beginning of the bit cell and another transition at the center of the bit cell, while a data bit of one is represented by a transition at the beginning of the bit cell only. These transitions may be of either polarity.

Bit combination 110 selects Biphase-Level decoding. In Biphase-Level, a data bit of zero is represented by a logic 0 during the first half of the bit cell and a logic 1 during the second half of the bit cell, while a data bit of one is represented by a logic 1 during the first half of the bit cell and a logic 0 during the second half of the bit cell.

Bit combination 111 selects differential Biphase-Level decoding. In differential Biphase-Level, a data bit of zero is represented by a transition at the center of the bit cell, with the same polarity as the transition at the center of the preceding bit cell while a data bit of one is represented by a transition at the center of the bit cell with the opposite polarity from the transition at the center of the preceding bit cell. In both cases, there may be transitions at the beginning of the bit cell to set up the level required to make the correct transition at the center of the bit cell.

5.20.2 Receive CRC Polynomial Control Field

Bits 12 and 11 select the CRC polynomial to be used by the receive CRC checker.

The CRC may only be used in synchronous modes. All control bits pertaining to CRC are ignored in the asynchronous modes.

Bit combination 00 selects the 16-bit CRC-CCITT polynomial. In HDLC, HDLC Loop, and 802.3 modes, the remainder is checked against F0B8 hex, which is consistent with the transmitted CRC being preset to ones, and inverted before transmission. The receive CRC preset value must be set to preset to ones, for a correct remainder to be generated. All other modes check for a remainder of zero.

Bit combination 01 selects the 16-bit CRC-16 polynomial. All modes check for a remainder of zero.

Bit combination 10 selects the 32-bit Ethernet polynomial. In HDLC, HDLC Loop, and 802.3 modes, the remainder is checked against C704DD7B hex, which is consistent with the transmitted CRC being preset to ones, and inverted before transmission. The receive CRC preset value must be set, to preset to ones, for a correct remainder to be generated. All other modes check for a remainder of zero.

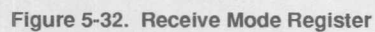
Bit combination 11 is reserved.

5.20.3 Receive CRC Preset Value Control Bit

Bit 10 is used to select the preset value for the receive CRC checker.

0 in this bit selects a reset value of all zeros for the receive CRC checker.

1 in this bit selects a reset value of all ones for the receive CRC checker. The CRC checker should always be preset to ones in HDLC, HDLC Loop, and 802.3 modes, to allow proper checking of the remainder, due to the fact that CRC is inverted before transmission in these modes.



5.20.4 Receive CRC Enable Control Bit

Bit 9 is used to enable and disable the receive CRC checker.

The state of this bit may be changed at any time, but the change only takes affect on character boundaries. In all synchronous modes, there is a one-character delay in the path between the data into the receive FIFO and the input to the receive CRC checker. This allows a specific character to be included or excluded from the CRC calculation. To do this, however, the FIFO cannot be used as only one character time is available to make the enable/disable decision. This one-character delay does not exist in HDLC and HDLC Loop modes because all data between the opening and closing flags should be included in the CRC calculation anyway.

The receive CRC checker is automatically reset when the receiver exits the hunt mode, so no user intervention is ever required.

While this bit is 0, any characters received will be excluded from the CRC calculation.

While this bit is 1, any characters received will be included in the CRC calculation.

5.20.5 Reserved Bit

Bit 8 is reserved.

5.20.6 Receive Parity Sense Control Field

Bits 7 and 6 are used to select the type of parity to be checked for in the receive data.

These bits are ignored unless parity is enabled. In the asynchronous modes, the parity bit is appended to the programmed character length, while in synchronous modes the parity bit is included in the programmed character length.

Bit combination 00 selects even parity. That is, there must be an even number of ones in the combination of data and parity bits.

Bit combination 01 selects odd parity. That is, there must be an odd number of ones in the combination of data and parity bits.

Bit combination 10 selects space parity. That is, there will be a zero in the parity bit location.

Bit combination 11 selects mark parity. That is, there will be a one in the parity bit location.

5.20.7 Receive Parity Enable Control Bit

Bit 5 is used to enable and disable the receive parity.

This bit should not be changed during reception of a character. The results are unpredictable when this occurs.

0 in this bit disables the receive parity checker.

1 in this bit enables the receive parity checker.

5.20.8 Receive Character Length Control Field

Bits 4 through 2 are used to select the receive character length.

The receive character length may not be changed on the fly as the internal data paths are character length dependent. Character length may be changed between characters in the asynchronous modes and while the receiver is in hunt in all synchronous modes.

One is automatically added to the programmed character length in the asynchronous modes if parity is enabled. Receive data is always right-justified in the RDR except in the case where the last byte of an HDLC frame is smaller than the programmed character length. In this case, where there is a non-zero residue code, the residual bits are left-justified in the RDR.

Bit combination 000 selects a character length of eight bits.

Bit combination 001 selects a character length of one bit.

Bit combination 010 selects a character length of two bits.

Bit combination 011 selects a character length of three bits.

Bit combination 100 selects a character length of four bits.

Bit combination 101 selects a character length of five bits.

Bit combination 110 selects a character length of six bits.

Bit combination 111 selects a character length of seven bits.

5.20.9 Receive Enable Control Field

Bits 1 and 0 are used to enable and disable the receiver.

Bit combination 00 disables the receiver immediately. Any data being received is lost.

Bit combination 01 disables the receiver after the current message, character or frame has been completed. In asynchronous modes the character being assembled is received, with parity and stop bits, before the receiver is disabled. In synchronous modes other than HDLC and 802.3, the message being received is completed before the receiver is disabled. In HDLC and 802.3 modes, the frame being received is completed before the receiver is disabled.

Bit combination 10 enables the receiver without the auto-enable feature. In this mode, the state of the /DCD pin has no effect on the receiver.

Bit combination 11 enables the receiver with the auto-enable feature turned on. In this mode, the /DCD pin acts as another enable for the receiver. The receiver is not enabled until the /DCD pin goes Low and remains Low. When the /DCD pin goes High in this mode the receiver is disabled in the same manner as if bit combination 00 had been programmed into these bits.

5.21 RECEIVE COMMAND/STATUS REGISTER

The Receive Command/Status register (RCSR) contains commands and status for the receiver (Figure 5-33).

5.21.1 Receive Command Field

Bits 15 through 12 are encoded with the commands for the receiver as shown below:

Bit combination 0000 is a Null command and has no effect on the receiver.

Bit combination 0001 is reserved.

Bit combination 0010 is the Preset CRC command. This command presets the receive CRC checker to the value programmed in the RMR. This command is not normally needed because the receiver automatically presets the CRC at the appropriate time at the beginning of a frame or message.

Bit combination 0011 is the Enter Hunt command. This command forces the receive microcode to jump to a particular address, independent of the mode the receiver is in. In the synchronous and HDLC modes, this has the effect of forcing the receiver into the hunt mode, where it will search for a sync or flag character to establish synchronization. In the asynchronous modes, any character assembly in progress is terminated and the receiver will start looking for a start bit or code violation, as appropriate.

Bit combination 0100 is reserved.

Bit combination 0101 is the Select FIFO Status command. This command enables the current number of bytes in the FIFO to be read in the upper byte of the RICR. This mode remains in effect until changed by another select FIFO receive command. The FIFO fill level is read-only. Writes to the upper byte of the RICR in this mode are ignored. Reset selects this mode for the RICR.

Bit combination 0110 is the select FIFO interrupt level command. This command enables the FIFO interrupt level to be accessed in the upper byte of the RICR. This mode remains in effect until changed by another select FIFO receive command. The FIFO interrupt level may be read and written in the upper byte of the RICR.

Bit combination 0111 is the select FIFO request level command. This command enables the FIFO request level to be accessed in the upper byte of the RICR. This mode remains in effect until changed by another select FIFO receive command. The FIFO request level may be read and written in the upper byte of the RICR.

Bit combinations 1000 through 1111 are reserved.

5.21.2 Second Byte in Error Status Bit

Bit 15 reports the error status of the byte immediately below the top of the FIFO.

This bit is updated at the time of an RDR read to reflect any error status present for the byte that is the second from the top of the FIFO at the time of the read. This status information is necessary when Status on Words is selected in the RICR and words are read from the RDR to decide which byte is in error. This bit will be set if the second byte received has an associated error, irrespective of whether straight or swapped memory data is selected via command in the CCAR.

This bit is updated whether the byte is valid or not in the FIFO so care must be exercised when using this information.

This bit is set to 1 if this second received byte is marked with a parity error, an overrun error or the CV/EOT/EOF bit set to 1; and is 0 otherwise.

5.21.3 First Byte in Error Status Bit

Bit 14 reports the error status of the byte at the top of the FIFO.

Address: 10010

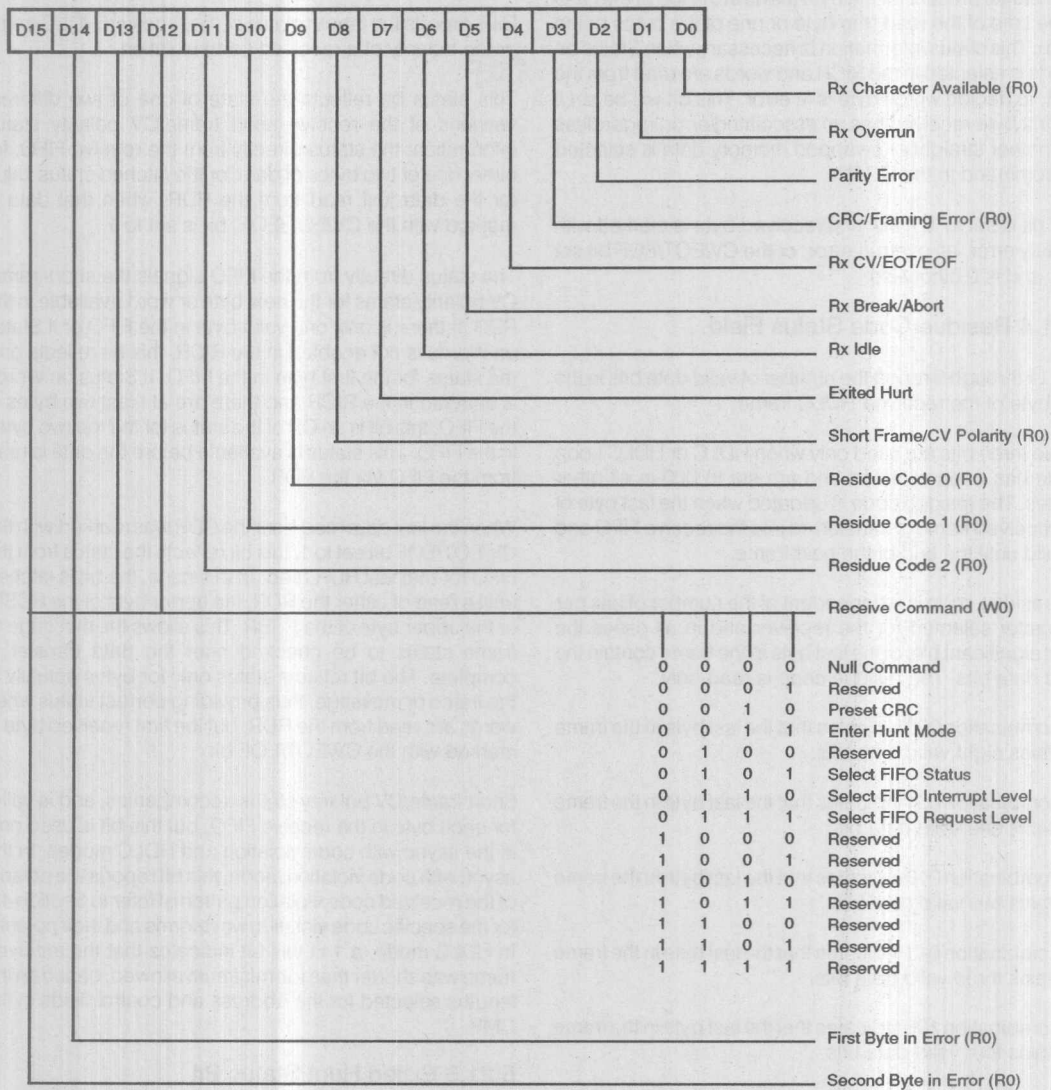


Figure 5-33. Receive Command/Status Register

This bit is updated at the time of an RDR read to reflect any error status present for the byte that is at the top of the FIFO at the time of the read (the byte or one of the bytes being read). This status information is necessary when Status on Words is selected in the RICR and words are read from the RDR, to decide which byte is in error. This bit will be set if the first byte received has an associated error, regardless of whether straight or swapped memory data is selected via command in the CCAR.

This bit is set to 1, if this first received byte is marked with a parity error, an overrun error, or the CV/EOT/EOF bit set to 1; and is 0 otherwise.

5.21.4 Residue Code Status Field

Bits 11 through 9 report the number of valid data bits in the last byte of the received HDLC frame.

These three bits are used only when HDLC or HDLC Loop mode has been selected and are set to 000 in all other modes. The residue code is updated when the last byte of the received frame is transferred into the receive FIFO and is valid until the end of the next frame.

The residue code is independent of the number of bits per character selected for the receiver and in all cases the most significant bits of the last byte in the frame contain the valid data bits. The residue code is read-only.

Bit combination 000 indicates that the last byte in the frame contains eight valid data bits.

Bit combination 001 indicates that the last byte in the frame contains one valid data bit.

Bit combination 010 indicates that the last byte in the frame contains two valid data bits.

Bit combination 011 indicates that the last byte in the frame contains three valid data bits.

Bit combination 100 indicates that the last byte in the frame contains four valid data bits.

Bit combination 101 indicates that the last byte in the frame contains five valid data bits.

Bit combination 110 indicates that the last byte in the frame contains six valid data bits.

Bit combination 111 indicates that the last byte in the frame contains seven valid data bits.

5.21.5 Short Frame/CV Polarity Status Bit

Bit 8 reports the length status of the received HDLC frame or the polarity of a received code violation.

This status bit reflects the state of one of two different versions of the receive short frame/CV polarity status information: the status directly from the receive FIFO, for either one or two bytes of data, or the latched status value for the data just read from the RDR, when that data is marked with the CV/EOT/EOF, bit is set to 1.

The status directly from the FIFO signals the short frame/CV polarity status for the next byte or word available in the RDR. If there is only one valid byte in the FIFO or if Status on Words is not enabled in the RICR, this bit reflects only the status for the first byte in the FIFO. If Status on Words is enabled in the RICR and there are at least two bytes in the FIFO, this bit is an OR of the status for the top two bytes in the FIFO. This status is available before the data is read from the FIFO via the RDR.

When the last data read from the RDR was marked with the CV/EOT/EOF bit set to 1, this bit reflects the status from the FIFO for that last RDR read. In this case, the bit is latched until a read of either the RDR, the upper byte of the RCSR, or the upper byte of the RSBR. This allows the message or frame status to be checked after the data transfer is complete. The bit reflects status only for bytes actually in the frame or message, thus providing correct status when words are read from the RDR, but the first received byte is marked with the CV/EOT/EOF bit.

Short frame/CV polarity status accompanies, and is valid, for each byte in the receive FIFO, but this bit is used only in the async with code violation and HDLC modes. In the async with code violation mode, this bit reports the polarity of the received code violation pattern. Refer to Section 4.2 for the specific code violation waveforms and their polarity. In HDLC mode, a 1 in this bit indicates that the received frame was shorter than the minimum allowed, based on the lengths selected for the address and control fields in the CMR.

5.21.6 Exited Hunt Status Bit

Bit 7 reports the hunt mode status of the receiver.

This bit is set to 1 and latched when the receiver leaves the hunt mode. A receive status interrupt is generated if enabled in the RICR. Writing a 1 to this bit clears and opens this latch. No further Exited Hunt interrupts may be generated until this latch has been cleared.

0 in this bit indicates that the receiver has not yet exited the hunt mode.

The Exited Hunt status indication comes directly out of the receiver. Hunt mode is present in one form or another in all modes. In the asynchronous modes, the receiver leaves hunt immediately after being enabled. In external sync mode, the receiver exits hunt each time the sync signal is received, while in monosync and bisync it occurs when the sync character or characters have been recognized. In HDLC mode, the receiver exits hunt with the opening flag of each frame. In bisync transparent mode the receiver leaves hunt when SYN has been recognized and in 802.3 mode, a frame with an address match will cause the receiver to leave hunt mode.

5.21.7 Received Idle Status Bit

Bit 6 reports the idle status of the receiver.

This bit is set to 1 and latched when the receiver recognizes an idle line condition. A receive status interrupt is generated if enabled in the RICR. Writing a 1 to this bit clears and opens this latch. No further Received Idle interrupts may be generated until this latch has been cleared.

0 in this bit indicates that the idle line condition has not been received.

The idle line status indication comes directly out of the receiver. In all modes except HDLC the idle line is defined as sixteen consecutive ones, received at the receive clock rate. In HDLC mode, the idle line condition is defined as fifteen consecutive ones. This bit will remain set for the duration of the idle line condition, even after the latch is reset, until the receiver receives a zero.

Because the receiver uses the receive clock to count the ones for the idle line detect, this bit is not useful in Asynchronous mode. In this mode, the Rx Idle IE bit should be reset to 0, and this latch never reset to prevent spurious Rx Status interrupts.

5.21.8 Received Break/Abort Status Bit

Bit 5 reports the reception of a break or an abort by the receiver.

This bit is set to 1 and latched when either a break or an abort condition is recognized by the receiver. A receive status interrupt is generated if enabled in the RICR. Writing a 1 to this bit clears and opens this latch. No further Received Break/Abort interrupts may be generated until this latch has been cleared.

0 in this bit indicates that no break or abort has been received.

The Break/Abort status indication comes directly out of the receiver. In asynchronous modes, this bit reports only break status, which occurs when the receiver sees consecutive zeros for the start bit, the data and optional parity, and the stop bit. This bit will remain set for the duration of the break condition, even after the latch is reset, until the receiver receives a one. No interrupt will be generated at the termination of the break, and no characters are loaded into the FIFO as a result of the break. In HDLC mode, this bit reports reception of an abort, which is seven consecutive ones.

5.21.9 Received CV/EOT/EOF Status Bit

Bit 4 reports the reception of a Code Violation (CV), an End-Of-Frame (EOF) or an End-Of-Transmission (EOT) by the receiver.

This status bit reflects the state of one of three different versions of the received CV/EOT/EOF status information: the status directly from the receive FIFO, for either one or two bytes of data, a 1 if the data just read from the RDR was marked with this bit set to 1, and the latched status in the case where the Rx CV/EOT/EOF receive status interrupt is enabled.

The status directly from the FIFO signals that the next byte or word available in the RDR is marked with a CV/EOT/EOF status indication. If there is only one valid byte in the FIFO, or if Status on Words is not enabled in the RICR, this bit reflects only the status for the first byte in the FIFO. If Status on Words is enabled in the RICR and there are at least two bytes in the FIFO, this bit is an OR of the status for the top two bytes in the FIFO. This status is available before the data is read from the FIFO via the RDR.

When the last data read from the RDR is marked with this bit set to 1, the bit is held at 1 until a read of either the RDR, the upper byte of the RCSR, or the upper byte of the RSBR. This allows the message or frame status to be checked after the data transfer is complete. The First Byte in Error and Second Byte in Error status bits in this register may then be used to determine the last byte in the frame or message in the case of word reads of the RDR.

If the Rx CV/EOT/EOF IE bit in the RICR is set to 1, this bit is set to 1, and a receive status interrupt is generated, when the byte marked with CV/EOT/EOF status is read from the RDR. Writing a 1 to this bit clears and opens this latch. No further Rx CV/EOT/EOF status interrupts may be generated until this latch has been cleared.

The CV/EOT/EOF status is used only in external sync, async with code violations, HDLC, bisync transparent and 802.3 modes. In the external sync mode, the character being assembled when the /DCD signal goes inactive is marked with this status in the FIFO. In the async with code violations mode, all characters are marked with this status if the Receive Extended Word option is not enabled in the CMR; if this option is enabled, only the second byte in the extended word is marked with this status. The last byte in the frame is marked with this bit in HDLC mode. In bisync transparent mode ETX, ITB, ETB, EOT and ENQ are all marked with this status, and in the 802.3 mode the last byte in the frame is marked with this status.

5.21.10 CRC/Framing Error Status Bit

Bit 3 reports the reception of either a CRC or framing error.

This status bit reflects the state of one of two different versions of the receive CRC/framing error status information: the status directly from the receive FIFO, for either one or two bytes of data, or the latched status value for the data just read from the RDR when that data is marked with the CV/EOT/EOF bit, is set to 1.

The status directly from the FIFO signals that the next byte or word available in the RDR is marked with a CRC/framing error status indication. If there is only one valid byte in the FIFO or if Status on Words is not enabled in the RICR, this bit reflects only the status for the first byte in the FIFO. If Status on Words is enabled in the RICR and there are at least two bytes in the FIFO, this bit is an OR of the status for the top two bytes in the FIFO. This status is available before the data is read from the FIFO via the RDR.

When the last data read from the RDR was marked with the CV/EOT/EOF bit set to 1, this bit reflects the status from the FIFO for that last RDR read. In this case, the bit is latched until a read of either the RDR, the upper byte of the RCSR, or the upper byte of the RSBR. This allows the message or frame status to be checked after the data transfer is complete. The bit reflects status only for bytes actually in the frame or message, thus providing correct status when words are read from the RDR, but the first received byte is marked with the CV/EOT/EOF bit.

Receive CRC/framing error status accompanies, and is valid, for each byte in the receive FIFO. In asynchronous modes this bit reports only framing error status, which occurs when a valid stop bit is not present with the data. In all synchronous modes this bit reports the result of the CRC calculation. In HDLC and 802.3 modes the CRC result indicated includes the byte it accompanies in the FIFO,

while in the other synchronous modes this CRC result includes neither the byte it accompanies in the FIFO nor the byte preceding it in the FIFO. Thus, to check the CRC result through a particular byte, both that byte and the succeeding byte must be read from the FIFO before the CRC status is available.

5.21.11 Parity Error Command/Status Bit

Bit 2 reports the parity error status of the receiver.

This status bit reflects the state of one of three different versions of the receive parity error status information: the status directly from the receive FIFO, for either one or two bytes of data, the latched status value for the data just read from the RDR when that data is marked with the CV/EOT/EOF bit is set to 1 and the latched status in the case where the Rx Overrun receive status interrupt is enabled.

The status directly from the FIFO signals that the next byte or word available in the RDR is marked with a parity error status indication. If there is only one valid byte in the FIFO, or if Status on Words is not enabled in the RICR, this bit reflects only the status for the first byte in the FIFO. If Status on Words is enabled in the RICR and there are at least two bytes in the FIFO, this bit is an OR of the status for the top two bytes in the FIFO. This status is available before the data is read from the FIFO via the RDR.

When the last data read from the RDR was marked with the CV/EOT/EOF bit set to 1, this bit reflects the status from the FIFO for that last RDR read. In this case, the bit is latched until a read of either the RDR, the upper byte of the RCSR, or the upper byte of the RSBR. This allows the message or frame status to be checked after the data transfer is complete. The bit reflects status only for bytes actually in the frame or message, thus providing correct status when words are read from the RDR, but the first received byte is marked with the CV/EOT/EOF bit.

If the Rx Parity Error IE bit in the RICR is set to 1, this bit is set to 1, and a receive status interrupt is generated, when the byte marked with parity error status is read from the RDR. Writing a 1 to this bit clears and opens this latch. No further Rx Parity Error status interrupts may be generated until this latch has been cleared.

Receive parity error status accompanies, and is valid, for each byte in the receive FIFO. Receive parity error occurs when receive parity is enabled in the RMR and the received character does not have parity matching the programmed sense. The parity error status will not be available until all of the valid data has been read from the FIFO, so that the parity error status is at the top of the FIFO.

5.21.12 Receive Overrun Command/Status Bit

Bit 1 reports the overrun status of the receive FIFO.

This status bit reflects the state of one of three different versions of the receive overrun status information: the status directly from the receive FIFO, for either one or two bytes of data, the latched status value for the data just read from the RDR when that data is marked with the CV/EOT/EOF, bit is set to 1, and the latched status in the case where the Rx Overrun receive status interrupt is enabled.

The status directly from the FIFO signals that the next byte or word available in the RDR is marked with an overrun status indication. If there is only one valid byte in the FIFO, or if Status on Words is not enabled in the RICR, this bit reflects only the status for the first byte in the FIFO. If Status on Words is enabled in the RICR, and there are at least two bytes in the FIFO, this bit is an OR of the status for the top two bytes in the FIFO. This status is available before the data is read from the FIFO via the RDR.

When the last data read from the RDR was marked with the CV/EOT/EOF bit set to 1, this bit reflects the status from the FIFO for that last RDR read. In this case, the bit is latched until a read of either the RDR, the upper byte of the RCSR, or the upper byte of the RSBR. This allows the message or frame status to be checked after the data transfer is complete. The bit reflects status only for bytes actually in the frame or message, thus providing correct status when words are read from the RDR, but the first received byte is marked with the CV/EOT/EOF bit.

If the Rx Overrun IE bit in the RICR is set to 1, this bit is set to 1, and a receive status interrupt is generated, when the byte marked with overrun status is read from the RDR. Writing a 1 to this bit clears and opens this latch. No further Rx Underrun status interrupts may be generated until this latch has been cleared.

Receive overrun status accompanies, and is valid, for each byte in the receive FIFO. Receive overrun occurs when the receive FIFO is full and another byte is written to the FIFO, writing over previous data. Once an overrun has occurred, no further writes to the FIFO are performed until a Receive FIFO Purge command is issued in the CCAR. The overrun status will not be available until all of the valid data has been read from the FIFO, so that the overrun status is at the top of the FIFO.

5.21.13 Receive Character Available Status Bit

Bit 0 reports the non-empty status of the receive FIFO.

This bit is read-only.

0 in this bit indicates that the receive FIFO is completely empty.

1 in this bit indicates that the receive FIFO contains at least one byte of receive data.

5.22 RECEIVE INTERRUPT CONTROL REGISTER

The Receive Interrupt Control register (RICR) contains control bits for the receiver. The upper byte controls the interrupt and DMA request levels of the FIFO and reports the current fill level of the FIFO, while the lower byte contains the IE bits for the sources of receive status interrupts (Figure 5-34).

5.22.1 Receive FIFO Control and Status Field

Bits 15 through 8 are used for receive FIFO control and status, with the exact function depending on the mode selected by a command in the RCSR.

After the Select FIFO Status command in the RCSR, this byte reports the number of bytes present in the receive FIFO. A value if "n" in this byte indicates that "n" bytes are present in the FIFO. This FIFO status is read-only. This is the reset selection.

After the Select FIFO Interrupt Level command in the RCSR, this byte controls the number of bytes which must be present in the receive FIFO before an interrupt request will be generated. A value "n" in this byte indicates that "n+1" bytes must be present in the FIFO before the interrupt request will be generated. This value may be read and written.

After the Select FIFO Request Level command in the RCSR, this byte controls the number of bytes which must be present in the receive FIFO before a DMA request will be generated. A value of "n" in this byte indicates that "n+1" bytes must be present in the FIFO before the DMA request will be generated. This value may be read and written.

5.22.2 Exited Hunt Interrupt Enable Control Bit

Bit 7 is used to control receive status interrupts when the receiver exits the hunt mode.

0 in this bit inhibits the generation of a receive status interrupt when the receiver exits the hunt mode.

1 in this bit enables the generation of a receive status interrupt when the receiver exits the hunt mode.

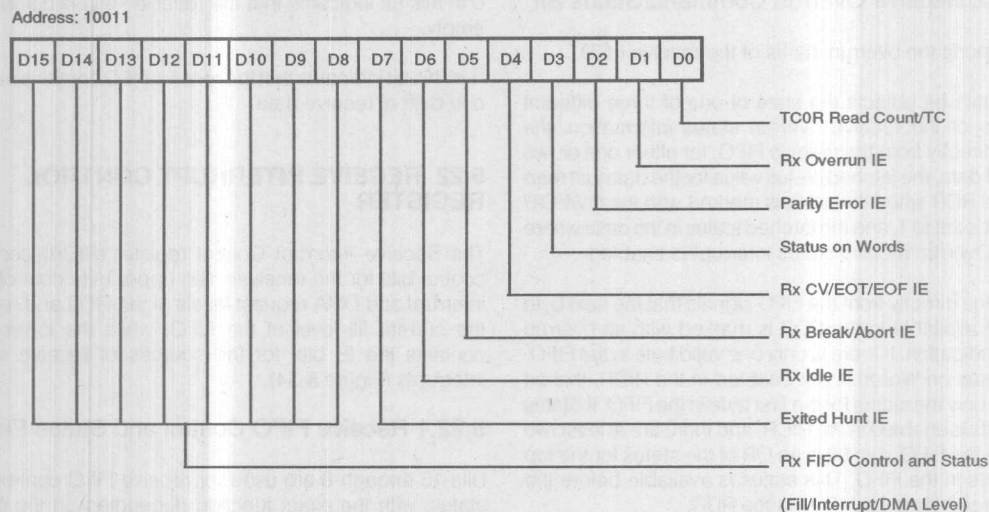


Figure 5-34. Receive Interrupt Control Register

5.22.3 Receive Idle Interrupt Enable Control Bit

Bit 6 is used to control idle line receive status interrupts.

0 in this bit inhibits the generation of a receive status interrupt when the receiver recognizes an idle line condition.

1 in this bit enables the generation of a receive status interrupt when the receiver recognizes an idle line condition.

5.22.4 Receive Break/Abort Interrupt Enable Control Bit

Bit 5 is used to control break and abort receive status interrupts.

0 In this bit inhibits the generation of a receive status interrupt when the receiver recognizes either a break or an abort condition.

1 in this bit enables the generation of a receive status interrupt when the receiver recognizes either a break or an abort condition.

5.22.5 Receive CV/EOT/EOF Interrupt Enable Control Bit

Bit 4 is used to control CV/EOT/EOF receive status interrupts.

0 in this bit inhibits the generation of a receive status interrupt when a character marked with the CV/EOT/EOF status is read from the receive FIFO.

1 in this bit enables the generation of a receive status interrupt when a character marked with the CV/EOT/EOF status is read from the receive FIFO.

5.22.6 Status On Words Control Bit

Bit 3 is used to control the way status information is presented in the RCSR and how receive status interrupts are generated in response to RDR reads.

0 In this bit selects status and interrupts on bytes. Only the status of the first byte in the receive FIFO will be reflected in the RCSR and reading the RDR will only generate a receive status interrupt if the first byte in the FIFO has an error condition.

1 in this bit selects status and interrupts on words. The status of the first two bytes in the receive FIFO will be reflected in the RCSR and reading the RDR will generate a receive status interrupt if either of the first two bytes in the FIFO have an error condition.

Reads of the RDR using either the D//C signal or the /RxAck signal are always the width of the data bus for the device; one byte for an eight bit bus and two bytes for the 16-bit bus. Thus, this bit must be set appropriately when using these facilities for data transfer. Data transfers using either a latched address, the pointer, or a separate address may be one byte, even in the 16-bit bus case.

5.22.7 Receive Parity Error Interrupt Enable Control Bit

Bit 2 is used to control parity error receive status interrupts.

0 in this bit inhibits the generation of a receive status interrupt when a character marked with parity error status is read from the receive FIFO.

1 in this bit enables the generation of a receive status interrupt when a character marked with parity error status is read from the receive FIFO.

5.22.8 Receive Overrun Interrupt Enable Control Bit

Bit 1 is used to control FIFO overrun receive status interrupts.

0 in this bit inhibits the generation of a receive status interrupt when a character marked with overrun error status is read from the receive FIFO.

1 in this bit enables the generation in a receive status interrupt when a character marked with overrun error status is read from the receive FIFO.

5.22.9 TCOR Read Count/TC Control Bit

Bit 0 is used to control the data read from the TCOR.

0 in this bit selects reads of the TCOR to return the time-constant that was written to the TCOR. This is the reset selection.

1 in this bit selects the current value in the counter to be read in TCOR. The count is not read asynchronously, but rather is frozen whenever this bit is written with a 1. Thus, to read the correct current count, the read of TCOR must be preceded by writing this bit with a 1.

5.23 RECEIVE SYNC REGISTER

The Receive Sync register (RSR) holds the sync character or characters for the transmitter in monosync and bisync modes and the station address in HDLC and 802.3 modes (Figure 5-35).

Sync and address characters held in this byte are always received least-significant bit first (either RSYN<0> or RSYN<8>), irrespective of the reception order option selected in the CCAR. Sync characters that are less than eight bits long must be right-justified in each byte of this register, with the most significant bit duplicated in the unused high-order bits.

In monosync mode, the single-sync character is held in the upper byte of this register.

In bisync mode, the lower byte holds Syn0, which is received first, while the upper byte holds Syn1, which is received second. If the Receive Sync Strip option is programmed in the CMR, the receiver will automatically strip all received Syn1 characters from the data stream. Syn0 characters will still be transferred to the FIFO in this case.

In HDLC mode the single-byte station address for address compare is held in the lower byte of this register.

In 802.3 mode, the 16-bit station address is held in this register, with RSYN<0> received first.

Address: 10100

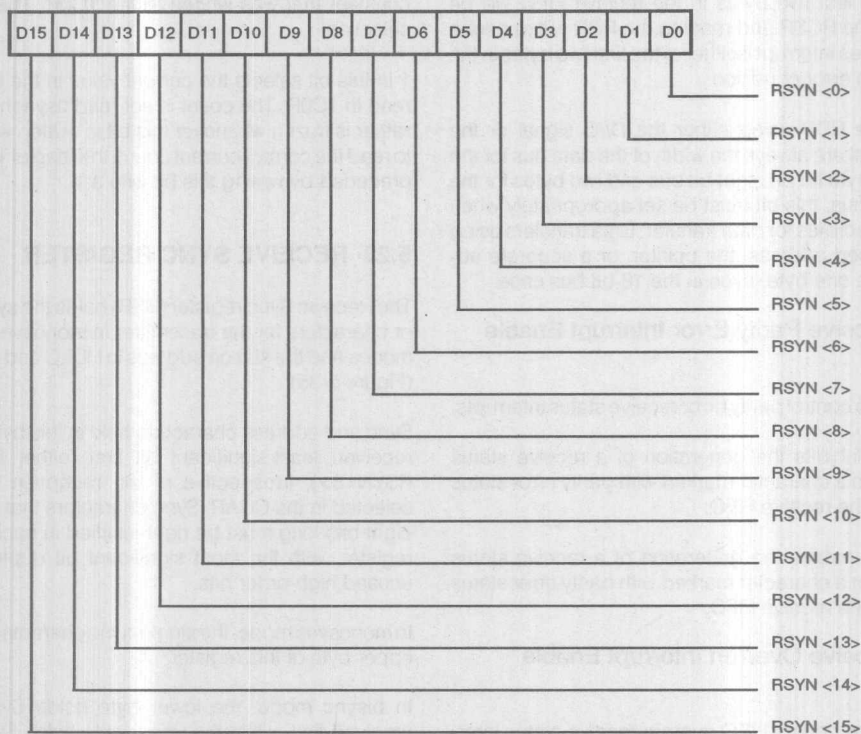


Figure 5-35. Receive Sync Register

5.24 RECEIVE COUNT LIMIT REGISTER

The Receive Count Limit Register (RCLR) holds the starting count value for the receive character counter (Figure 5-36).

Receive character counting operation is disabled while this register contains all zeros. A non-zero value in this register indicates the maximum allowable number of bytes of data to be received in this frame or message. The number in this register is the number of data bytes only; it does not include the number of bytes in the receive status block, if any.

Any receive character counting operation in progress is unaffected by writing a new value to this register, even if the new value is zero, which disables the character counting operation.

Writing a non-zero value to this register does not, in itself, enable the receive character counting operation. Rather, character counting operation is enabled or disabled and the receive character counter is loaded, either by the trigger receive DMA command, the reload receive character count command, the receive FIFO purge command, or receipt of an opening flag or sync character.

Writing this register with all ones allows the length of the frame or message to be easily determined; it is just the ones complement of the value in the RCCR or the RCHR.

The current count value may be read in the RCCR. The second word of the receive status block, if used, is the current value in the receive character count holding register (RCHR).

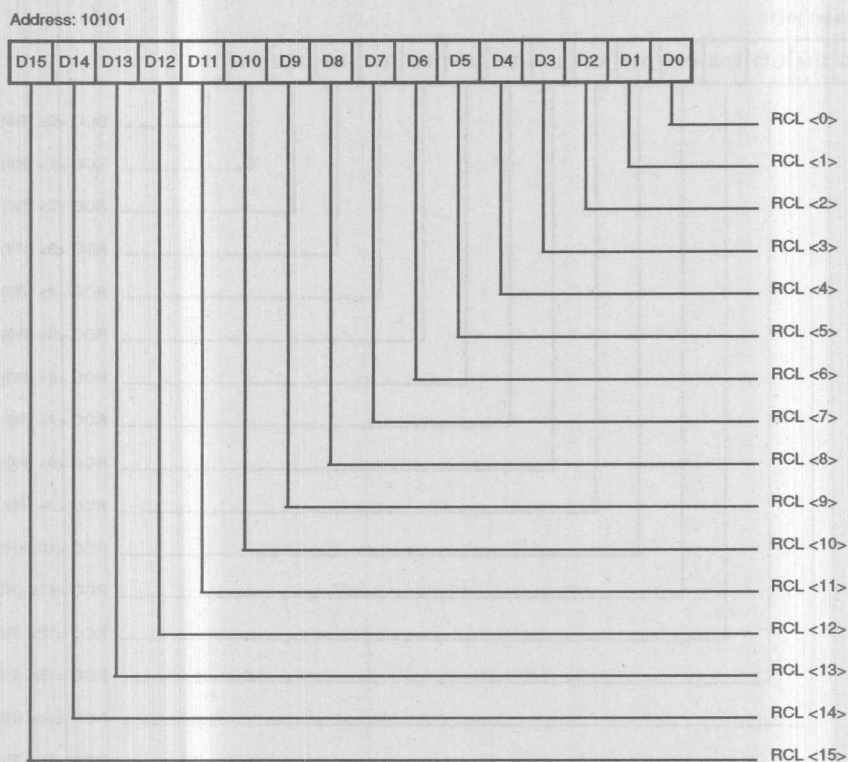


Figure 5-36. Receive Count Limit Register

5.25 RECEIVE CHARACTER COUNT REGISTER

The Receive Character Count Register (RCCR) contains the word at the top of the receive character count FIFO (Figure 5-37).

The RCC FIFO is four words deep and reports the status of the receive character counter. The RCC FIFO is written, along with the RCHR, with the contents of the receive character counter upon receipt of a closing flag or sync character. The top entry in the RCC FIFO is removed by a word read of the RCCR or by a byte read of the upper byte of the RCCR, and the RCC FIFO may be purged by command in the CCSR.

The receive character counter is loaded with the value in the RCLR, either by command or automatically upon

receipt of an opening flag or sync character. The receive character counter is decremented by one with each transfer from the receive shift register to the receive FIFO. Upon receipt of a closing flag or sync character, the contents of the receive character counter are transferred to the RCC FIFO and to the RCHR. This value may be used later to determine message or frame boundaries in the data transferred to memory. The count value held in the RCHR may also be transferred to memory as part of the receive status block.

If the RCLR is loaded with all ones, the value in the RCC FIFO is the one's complement of the number of characters transferred to memory in the frame or message, or the value in the RCLR may be used to limit the maximum length of received frames or messages, since an interrupt may be programmed if the receive character counter tries to decrement from a count of zero.

Address: 10110

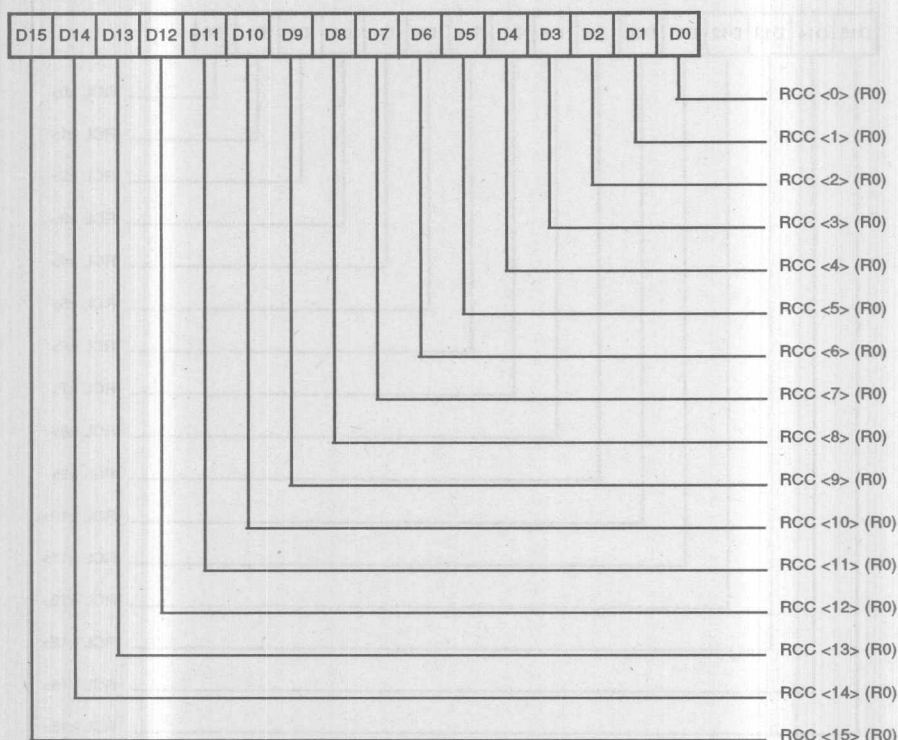


Figure 5-37. Receive Character Count Register

5.26 TIME CONSTANT 0 REGISTER

The Time Constant 0 Register (TCOR) holds the time constant used by baud rate generator 0 (Figure 5-38).

The TCOR is a read/write register but the value returned during a read depends on the state of the TCOR Read Count/TC control bit in the RICR. If the TCOR Read Count/TC control bit in the RICR is set to zero, the time constant is returned during the read; otherwise the current count in the counter is returned.

The counter in the baud rate generator automatically reloads the time constant when a count of zero is reached in continuous mode, and stops at the count of zero when operating in the single-cycle mode. The time constant may be loaded into the counter with a command in the CCAR.

The baud rate generator divides its input clock by the value of the time constant, plus one, to provide the baud rate generator output. The output of the baud rate generator is always a square wave.

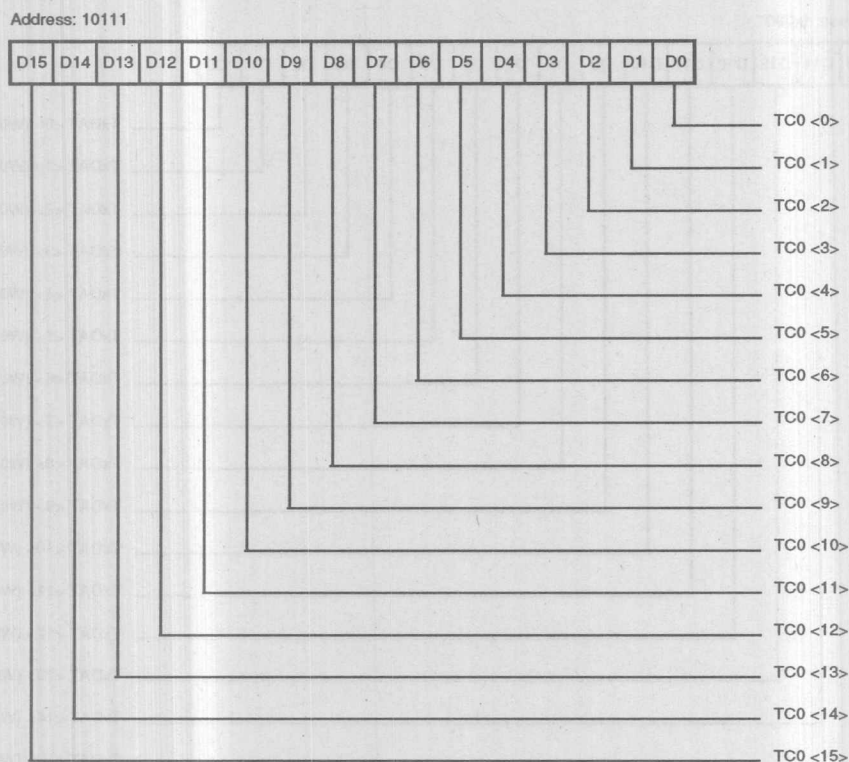


Figure 5-38. Time Constant 0 Register

5.27 TRANSMIT DATA REGISTER

The Transmit Data Register (TDR) is the input to the transmit FIFO (Figure 5-39).

The TDR is a write-only register. Data may be read from the top of the transmit data FIFO with the appropriate test mode access. The TDR may be addressed by the address latched with the /AS signal, indirectly by the pointer in the CCAR, directly via the D//C pin active High, or directly through the /TxACK signal.

Either bytes or words may be written to the TDR. In the case of a byte write, the lower byte of the register must be used and internal logic will properly enter the data into the FIFO. In the case of a word write, the byte ordering into the FIFO must be initially specified by a command in the CCAR. In

the case of straight memory data, which is the default case, the most significant byte of the TDR (bits 8-15) will enter the FIFO first and thus be transmitted first, with the least significant byte (bits 0-7) entering the FIFO and being transmitted second. In the case of swapped memory data, the least significant byte of the TDR (bits 0-7) will enter the FIFO first and be transmitted first, with the most significant byte (bits 8-15) entering the FIFO and being transmitted second.

The data in the transmit FIFO is always transmitted least significant bit (bit 0) first, but the bit order may be programmably swapped at the input to the FIFO via a command in the CCAR. The default case is no swap (LSB first).

Address: 1x000

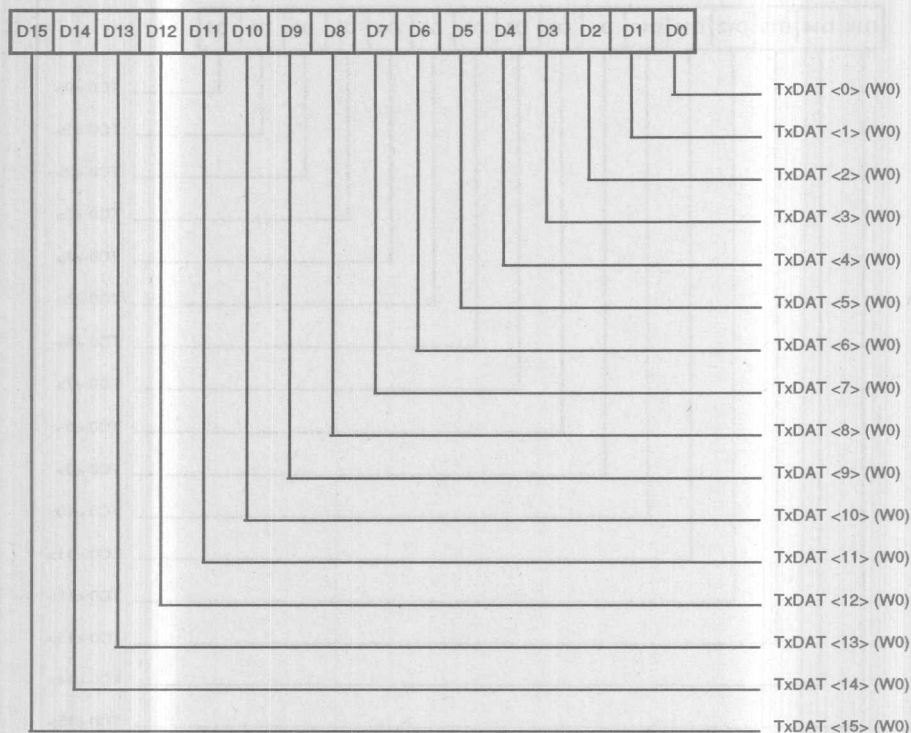


Figure 5-39. Transmit Data Register

5.28 TRANSMIT MODE REGISTER

The Transmit Mode Register (TMR) contains various control bits for the transmitter (Figure 5-40).

5.28.1 Transmit Data Encoding Control Field

Bits 15 through 13 are used to select the data encoding method used by the transmitter.

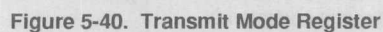
Bit combination 000 selects NRZ encoding. In NRZ, a data bit of zero is represented by a logic 0 for the duration of the bit cell, and a data bit of one is represented by a logic 1 for the duration of the bit cell.

Bit combination 001 selects NRZB encoding. In NRZB, a data bit of zero is represented by a logic 1 for the duration of the bit cell, and a data bit of one is represented by a logic 0 for the duration of the bit cell.

Bit combination 010 selects NRZI-Mark encoding. In NRZI-Mark, a data bit of zero is represented by no transition at the beginning of the bit cell, and a data bit of one is represented by a transition at the beginning of the bit cell. That is, the level present in the preceding bit cell is reversed for a one and continued for a zero.

Bit combination 011 selects NRZI-Space encoding. In NRZI-Space, a data bit of zero is represented by a transition at the beginning of the bit cell, and a data bit of one is represented by no transition at the beginning of the bit cell. That is, the level present in the preceding bit cell is reversed for a zero and continued for a one.

Bit combination 100 selects Biphas-Mark encoding. In Biphas-Mark, a data bit of zero is represented by a transition at the beginning of the bit cell only, and a data bit of one is represented by a transition at the beginning of the bit cell and another transition at the center of the bit cell. These transitions may be of either polarity.



Bit combination 101 selects Biphase-Space encoding. In Biphase-Space, a data bit of zero is represented by a transition at the beginning of the bit cell and another transition at the center of the bit cell, while a data bit of one is represented by a transition at the beginning of the bit cell only. These transitions may be of either polarity.

Bit combination 110 selects Biphase-Level encoding. In Biphase-Level, a data bit of zero is represented by a logic 0 during the first half of the bit cell and a logic 1 during the second half of the bit cell. A data bit of one is represented by a logic 1 during the first half of the bit cell and a logic 0 during the second half of the bit cell.

Bit combination 111 selects differential Biphase-Level encoding. In differential Biphase-Level, a data bit of zero is represented by a transition at the center of the bit cell, with the same polarity as the transition at the center of the preceding bit cell. A data bit of one is represented by a transition at the center of the bit cell with the opposite polarity from the transition at the center of the preceding bit cell. In both cases, there may be transitions at the beginning of the bit cell to set up the level required to make the correct transition at the center of the bit cell.

5.28.2 Transmit CRC Polynomial Control Field

Bits 12 and 11 select the CRC polynomial to be used by the transmit CRC generator.

The CRC may only be used in synchronous modes. All control bits pertaining to CRC are ignored in the asynchronous modes.

Bit combination 00 selects the 16-bit CRC-CCITT polynomial. The CRC is inverted before transmission in HDLC, HDLC Loop and 802.3 modes.

Bit combination 01 selects the 16-bit CRC-16 polynomial.

Bit combination 10 selects the 32-bit Ethernet polynomial. The CRC is inverted before transmission in HDLC, HDLC Loop and 802.3 modes.

Bit combination 11 is reserved.

5.28.3 Transmit CRC Preset Value Control Bit

Bit 10 is used to select the preset value for the transmit CRC generator.

0 in this bit selects a reset value of all zeros for the transmit CRC generator.

1 in this bit selects a reset value of all ones for the transmit CRC generator. As a result of the automatic inversion of

CRC before transmission in HDLC, HDLC Loop and 802.3 modes, the transmit CRC generator must be preset to all ones to allow proper checking of the remainder.

5.28.4 Transmit CRC Enable Control Bit

Bit 9 is used to enable and disable the transmit CRC generator.

The state of this bit is carried in the FIFO along with the data. This allows CRC to be enabled and disabled on a byte by byte basis while still utilizing the FIFO. The state of the bit at the time of the FIFO write is carried along with the data. Word writes to the transmit FIFO assign the state of this bit to both bytes entered into the FIFO.

While this bit is 0, any characters written to the transmit FIFO will not be included in the CRC calculation.

While this bit is 1, any characters written to the transmit FIFO will be included in the CRC calculation.

5.28.5 Transmit CRC on EOF/EOM Control Bit

Bit 8 is used to select the action of the transmitter after sending the last byte in the frame or message.

This bit is ignored in the asynchronous modes and functions in the synchronous modes irrespective of whether or not CRC has been enabled.

0 in this bit inhibits the transmitter from automatically sending the CRC after the byte marked as the last in the frame or message is transmitted. CRC may still be transmitted upon FIFO underrun, as programmed in the TCSR.

1 in this bit enables the transmitter to automatically send the CRC after the byte marked as the last in the frame or the message is sent. A byte in the transmit FIFO may be marked as the last byte, either by command in the TCSR or automatically when the transmit character counter has counted down to zero. The frame or message is then terminated as programmed by the Tx Underrun Condition bits in the CMR.

5.28.6 Transmit Parity Sense Control Field

Bits 7 and 6 are used to select the type of parity to be appended to transmit data.

These bits are ignored unless parity is enabled. In the asynchronous modes the parity bit is appended to the programmed character length, while in synchronous modes the parity bit is included in the programmed character length.

Bit combination 00 selects even parity. That is, there must be an even number of ones in the combination of data and parity bits.

Bit combination 01 selects odd parity. That is, there must be an odd number of ones in the combination of data and parity bits.

Bit combination 10 selects space parity. That is, there will be a zero in the parity bit location.

Bit combination 11 selects mark parity. That is, there will be a one in the parity bit location.

5.28.7 Transmit Parity Enable Control Bit

Bit 5 is used to enable and disable the transmit parity.

This bit should not be changed during transmission of a character. The results are unpredictable when this occurs.

0 in this bit disables the transmission of parity information.

1 in this bit enables the transmission of parity information.

5.28.8 Transmit Character Length Control Field

Bits 4 through 2 are used to select the transmit character length.

The transmit character length may be changed at any time. The new character length takes effect on the next character loaded into the transmit shift register. One is automatically added to the programmed character length in asynchronous modes if parity is enabled. The data bits must always be right-justified in the TDR.

Bit combination 000 selects a character length of eight bits.

Bit combination 001 selects a character length of one bit. One bit per character can only be selected in Asynchronous, Isochronous, Async with CV and NBIP modes.

Bit combination 010 selects a character length of two bits.

Bit combination 011 selects a character length of three bits.

Bit combination 100 selects a character length of four bits.

Bit combination 101 selects a character length of five bits.

Bit combination 110 selects a character length of six bits.

Bit combination 111 selects a character length of seven bits.

5.28.9 Transmit Enable Control Field

Bits 1 and 0 are used to enable and disable the transmitter.

Bit combination 00 disables the transmitter immediately. The transmitter immediately begins sending ones.

Bit combination 01 disables the transmitter after the current transmission has been completed. In asynchronous modes the character being transmitted is sent, with parity and stop bits, before the transmitter is disabled. In synchronous modes other than HDLC, HDLC Loop and 802.3, the message is completed before the transmitter is disabled. In HDLC, HDLC Loop and 802.3 modes, the frame being sent is closed appropriately before the transmitter is disabled. Continuous ones are sent while the transmitter is disabled in all modes.

Bit combination 10 enables the transmitter without the auto enable feature. In this mode, the state of the /CTS pin has no effect on the transmitter.

Bit combination 11 enables the transmitter with the auto enable feature turned on. In this mode, the /CTS pin acts as another enable for the transmitter. The transmitter is not enabled until the /CTS pin goes Low and remains Low. When the /CTS pin goes High in this mode, the transmitter is disabled in the same manner as if bit combination 00 had been programmed into these bits.

5.29 TRANSMIT COMMAND/STATUS REGISTER

The Transmit Command/Status Register (TCSR) contains commands and status for the transmitter (Figure 5-41).

5.29.1 Transmit Command Field

Bits 15 through 12 are encoded with the commands for the transmitter as shown below:

Bit combination 0000 is a Null command and has no effect on the transmitter.

Bit combination 0001 is reserved.

Bit combination 0010 is the Preset CRC command. This command presets the transmit CRC generator to the value programmed in the TMR. This command is not normally needed because the transmitter automatically presets the CRC at the appropriate time at the beginning of a frame or message.

Address: 11010

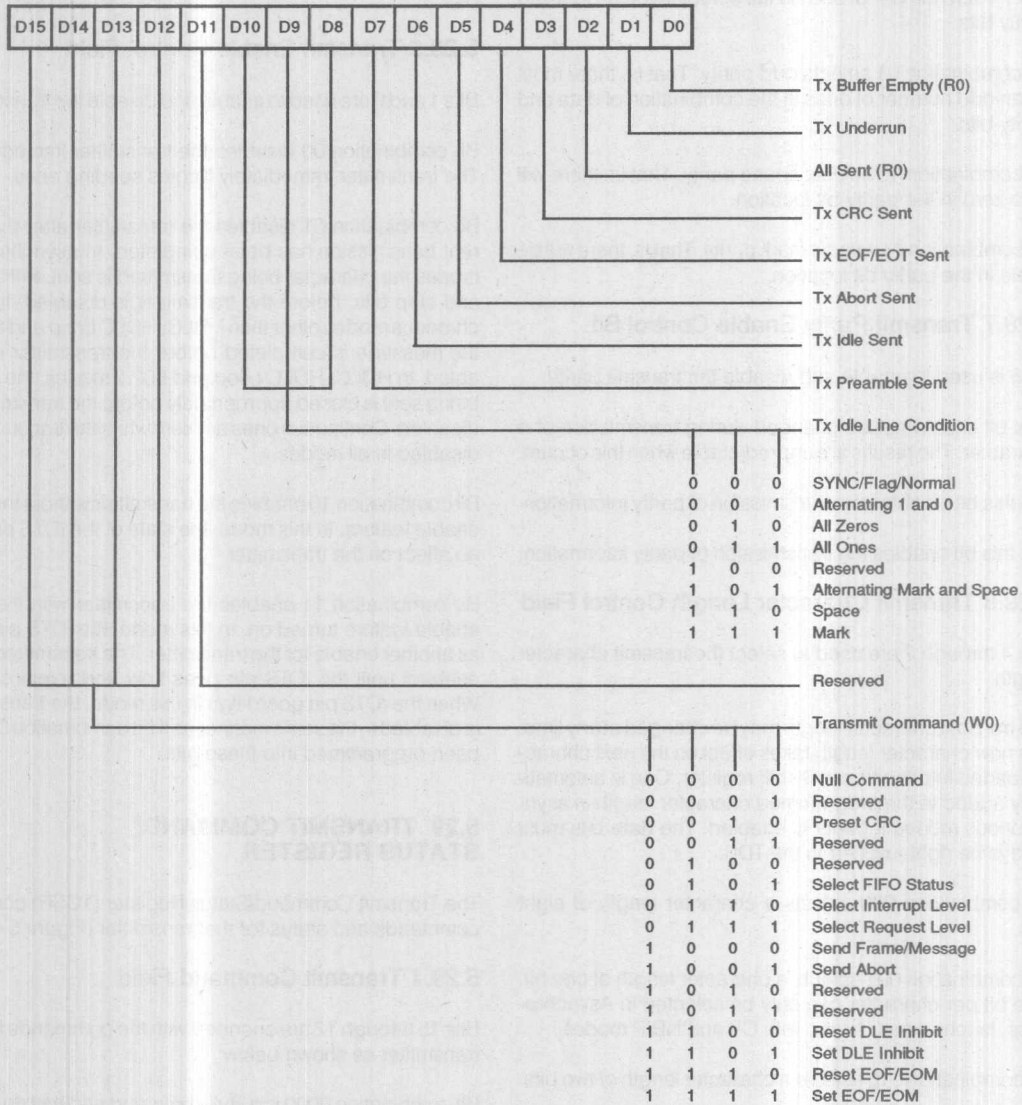


Figure 5-41. Transmit Command/Status Register

Bit combinations 0011 and 0100 are reserved.

Bit combination 0101 is the Select FIFO Status command. This command enables the current number of byte locations available in the FIFO to be read in the upper byte of the TICR. This mode remains in effect until changed by another select FIFO transmit command. The FIFO empty level is read-only. Writes to the upper byte of the TICR in this mode are ignored. Reset selects this mode for the TICR.

Bit combination 0110 is the Select FIFO Interrupt Level command. This command enables the FIFO interrupt level to be accessed in the upper byte of the TICR. This mode remains in effect until changed by another select FIFO transmit command. The FIFO interrupt level may be read and written in the upper byte of the TICR.

Bit combination 0111 is the Select FIFO Request Level command. This command enables the FIFO request level to be accessed in the upper byte of the TICR. This mode remains in effect until changed by another select FIFO transmit command. The FIFO request level may be read and written in the upper byte of the TICR.

Bit combination 1000 is the Send Frame/Message command. This command is used with the Wait for Send Command bit in the TICR to enable the transmitter to send the next frame or message after having completed the transmission of the previous frame or message. If the Wait For Send Command bit is not set in the TICR, this command has no effect on the transmitter.

Bit combination 1001 is the Send Abort command. This command is used only in HDLC mode to force the transmitter to send an abort. An abort is a zero followed by seven consecutive ones. If the Extended Abort bit in the CCR is set to 1, the abort is a zero followed by fourteen consecutive ones. The transmitter resumes normal operation upon completing transmission of the abort.

Bit combinations 1010 and 1011 are reserved.

Bit combination 1100 is the Reset DLE Inhibit command. This command is used only in the bisync transparent mode to reset the latch which controls the automatic insertion of DLE into the transmit data stream. When this latch is reset, the transmitter will automatically insert a DLE in front of a DLE in the transmit data. This is the default case.

Bit combination 1101 is the Set DLE Inhibit command. This command sets the latch which will inhibit the automatic insertion of DLE into the transmit data stream in front of a data DLE. This latch is not automatically reset after a write

to the TDR, but must be explicitly reset with the Reset DLE Inhibit command.

Bit combination 1110 is the Reset EOF/EOM command. This command clears the EOF bit which accompanies transmit data in the transmit FIFO. Thus, any data written to the FIFO after this command will not be marked as EOF. This is the default case.

Bit combination 1111 is the Set EOF/EOM command. This command sets the EOF bit, which accompanies transmit data in the transmit FIFO. The byte written to the FIFO immediately after this command is marked as EOF, but the bit is cleared automatically by a write to the TDR, so only this command needs be issued at the end of a frame or message. If a word is written to the TDR after this command is issued, only the byte on AD0-7 will be written to the FIFO and marked as the end-of-frame and any data on AD8-15 will be ignored.

5.29.2 Reserved Bit

Bit 11 is reserved.

5.29.3 Transmit Idle Line Condition Control Field

Bits 10 through 8 are used to select the idle line condition for the transmitter.

Bit combination 000 selects the normal idle line case, which is all ones in asynchronous and 802.3 modes, sync characters in synchronous modes and flags in HDLC and HDLC Loop modes. The selected data encoding method will apply during this idle line condition.

Bit combination 001 selects an idle line condition of alternating ones and zeros. The selected data encoding method applies to these ones and zeros, which allows a DPLL at the receiving end to maintain sync.

Bit combination 010 selects an idle line condition of all zeros. The selected data encoding method applies to these zeros.

Bit combination 011 selects an idle line condition of all ones. The selected data encoding method applies to these ones.

Bit combination 100 is reserved.

Bit combination 101 selects an idle line condition of alternating mark and space. Thus, the transmit data pin toggles between one and zero, irrespective of the selected data encoding method.

Bit combination 110 selects an idle line condition of space. In this case, the transmit data pin is Low while the transmitter is idle, irrespective of the selected data encoding method.

Bit combination 111 selects an idle line condition of mark. In this case, the transmit data pin is High while the transmitter is idle, irrespective of the selected data encoding method.

5.29.4 Transmit Preamble Sent Command/Status Bit

Bit 7 reports the status of the transmission of the preamble.

This bit is set to 1 and latched when the transmitter has completed transmission of the preamble. A transmit status interrupt is generated if enabled in the TICR. Writing a 1 to this bit clears and opens this latch. No further Preamble Sent interrupts may be generated until this latch has been cleared.

0 in this bit indicates that transmission of the preamble has not been completed. Writing a 0 to this bit has no effect.

The preamble pattern is programmed in the CCR.

5.29.5 Transmit Idle Sent Command/Status Bit

Bit 6 reports the status of the transmission of the idle line.

This bit is set to 1 and latched when the transmitter has completed transmission of the idle line. A transmit status interrupt is generated if enabled in the TICR. Writing a 1 to this bit clears and opens this latch. No further Idle Sent interrupts may be generated until this latch has been cleared.

0 in this bit indicates that transmission of the idle line has not been completed. Writing a 0 to this bit has no effect.

The idle line is defined by the Tx Idle Line Condition control field in this register.

5.29.6 Transmit Abort Sent Command/Status Bit

Bit 5 reports the status of the transmission of the abort.

This bit is set to 1 and latched when the transmitter has completed transmission of the abort. A transmit status interrupt is generated if enabled in the TICR. Writing a 1 to this bit clears and opens this latch. No further Abort Sent interrupts may be generated until this latch has been cleared.

0 in this bit indicates that transmission of the abort has not been completed. Writing a 0 to this bit has no effect.

The abort is used only in HDLC mode and is defined as seven consecutive ones, or fourteen consecutive ones if the Extended Abort bit in the CCR is set to 1.

5.29.7 Transmit EOF/EOT Sent Command/Status Bit

Bit 4 reports the status of the transmission of the closing flag or sync character.

This bit is set to 1 and latched when the transmitter has completed transmission of the closing flag or sync character. A transmit status interrupt is generated if enabled in the TICR. Writing a 1 to this bit clears and opens this latch. No further EOF/EOT Sent interrupts may be generated until this latch has been cleared.

A 0 in this bit indicates that transmission of the closing flag or sync character has not been completed. Writing a 0 to this bit has no effect.

5.29.8 Transmit CRC Sent Command/Status Bit

Bit 3 reports the status of the transmission of the CRC.

This bit is set to 1 and latched when the transmitter has completed transmission of the CRC. A transmit status interrupt is generated if enabled in the TICR. Writing a 1 to this bit clears and opens this latch. No further CRC Sent interrupts may be generated until this latch has been cleared.

0 in this bit indicates that transmission of the CRC has not been completed. Writing a 0 to this bit has no effect.

5.29.9 All Sent Status Bit

Bit 2 reports the status of the transmission of a character in asynchronous modes.

This bit is used only in asynchronous modes and is set to 0 in all other modes. This bit is read-only.

0 in this bit indicates that the entire async character has not yet reached the transmit data pin.

1 in this bit indicates that the stop bit has reached the transmit data pin and has been been completely sent.

5.29.10 Transmit Underrun Command/Status Bit

Bit 1 reports the underrun status of the transmit FIFO.

This bit is set to 1 and latched when the transmit FIFO underruns. A transmit status interrupt is generated if enabled in the TCSR. Writing a 1 to this bit clears and opens the latch. No further Tx Underrun interrupts may be generated until this latch has been cleared.

A 0 in this byte indicates that the transmit FIFO has not underrun. Writing a 0 to this bit has no effect.

Transmit underrun occurs when the transmit FIFO is empty and another byte is requested from the FIFO. Upon underrun, the transmitter begins sending an idle line, CRC, or a closing flag or sync character, as appropriate.

5.29.11 Transmit Buffer Empty Status Bit

Bit 0 reports the empty status of the transmit FIFO.

This bit is read-only.

A 0 in this bit indicates that the transmit FIFO contains at least one byte of transmit data.

1 in this bit indicates that the transmit FIFO is completely empty.

5.30 TRANSMIT INTERRUPT CONTROL REGISTER

The Transmit Interrupt Control Register (TICR) contains control bits for the transmitter. The upper byte controls the interrupt and DMA request levels of the FIFO and reports the current fill level of the FIFO, while the lower byte contains the IE bits for the sources of transmit status interrupts (Figure 5-42).

5.30.1 Transmit FIFO Control and Status Field

Bits 15 through 8 are used for transmit FIFO control and status, with the exact function depending on the mode selected by a command in the TCSR.

After the Select FIFO Status command in the TCSR, this byte reports the number of byte locations available in the transmit FIFO. A value of "n" in this byte indicates that "n" byte locations are available in the FIFO. This FIFO status is read-only. This is the reset selection.

After the Select FIFO Interrupt Level command in the TCSR, this byte controls the number of byte locations

which must be available in the transmit FIFO before an interrupt request will be generated. A value of "n" in this byte indicates that "n+1" byte locations must be available in the FIFO before the interrupt request will be generated. This value may be read and written.

After the Select FIFO Request Level command in the TCSR, this byte controls the number of byte locations which must be available in the transmit FIFO before a DMA request will be generated. A value of "n" in this byte indicates that "n+1" byte locations must be available in the FIFO before the DMA request will be generated. This value may be read and written.

5.30.2 Transmit Preamble Sent Interrupt Enable Control Bit

Bit 7 is used to control preamble sent transmit status interrupts.

0 in this bit inhibits a transmit status interrupt at the completion of the transmission of the preamble.

1 in this bit enables a transmit status interrupt at the completion of the transmission of the preamble. This interrupt is generated when the last bit of the preamble has been sent from the TxD pin.

5.30.3 Transmit Idle Sent Interrupt Enable Control Bit

Bit 6 is used to control idle sent transmit status interrupts.

0 in this bit inhibits a transmit status interrupt at the completion of the transmission of the idle line pattern.

1 in this bit enables a transmit status interrupt at the completion of the transmission of the idle line pattern. This interrupt is generated when the last bit of the idle line pattern has been sent from the TxD pin.

5.30.4 Transmit Abort Sent Interrupt Enable Control Bit

Bit 5 is used to control abort sent transmit status interrupts.

0 in this bit inhibits a transmit status interrupt at the completion of the transmission of the abort.

1 in this bit enables a transmit status interrupt at the completion of the transmission of the abort. This interrupt is generated when the last bit of the preamble has been sent from the TxD pin. Note that abort is transmitted only in HDLC and HDLC Loop modes.

Address: 11011

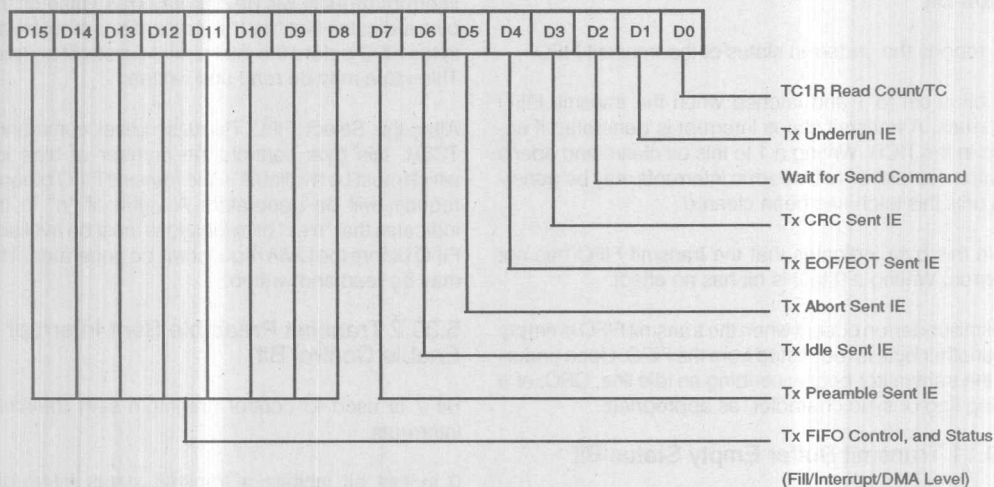


Figure 5-42. Transmit Interrupt Control Register

5.30.5 Transmit EOF/EOT Sent Interrupt Enable Control Bit

Bit 4 is used to control EOF/EOT sent transmit status interrupts.

0 in this bit inhibits a transmit status interrupt at the completion of the transmission of the closing flag or sync character.

1 in this bit enables a transmit status interrupt at the completion of the transmission of the closing flag or sync character. This interrupt is generated when the last bit of this flag or sync has been sent from the TxD pin.

5.30.6 Transmit CRC Sent Interrupt Enable Control Bit

Bit 3 is used to control CRC sent transmit status interrupts.

0 in this bit inhibits a transmit status interrupt at the completion of the transmission of the CRC.

1 in this bit enables a transmit status interrupt at the completion of the transmission of the CRC. This interrupt is generated when the last bit of the CRC has been sent from the TxD pin.

5.30.7 Wait for Send Command Control Bit

Bit 2 is used to control the action of the transmitter at the end of a transmitted frame or message.

0 in this bit allows the transmitter to proceed immediately with the transmission of another frame or message once there is more data in the transmit FIFO.

A 1 in this bit makes the transmitter wait for the Send Frame/Message command in the TCSR before starting transmission of another frame or message, even though data may be present in the transmit FIFO. The transmitter sends the idle line condition while waiting for this command. The command may be issued at any time after the last byte of the frame or message is removed from the transmit FIFO.

5.30.8 Transmit Underrun Interrupt Enable Control Bit

Bit 1 is used to control FIFO underrun transmit status interrupts.

0 in this bit inhibits a transmit status interrupt in response to a FIFO underrun condition.

1 in this bit enables a transmit status interrupt in response to a FIFO underrun condition.

5.30.9 TC1R Read Count/TC Control Bit

Bit 0 is used to control the data read from the TC1R.

0 in this bit selects reads of the TC1R to return the time constant that was written to the TC1R. This is the reset selection.

1 in this bit selects the current value in the counter to be read in TC1R. The count is not read asynchronously, but rather is frozen whenever this bit is written with a 1. Thus, to read the correct current count, the read of TC1R must be preceded by writing this bit with a 1.

5.31 TRANSMIT SYNC REGISTER

The Transmit Sync Register (TSR) holds the sync character or characters for the transmitter in monosync, bisync and slaved monosync modes (Figure 5-43).

Sync characters held in this register are always sent least significant bit first (either $TSYN<0>$ or $TSYN<8>$), irrespective of the transmission order option selected in the CCAR. Sync characters that are less than eight bits long must be right-justified in each byte of this register, with the unused bits ignored by the device.

In monosync and slaved monosync modes, the single-sync character is held in the lower byte of this register.

In bisync mode, the lower byte holds $Syn0$, which is transmitted first while the upper byte holds $Syn1$, which is transmitted second. The idle line and underrun condition may be programmed in the CMR to be either $Syn1$ alone or the $Syn0$ - $Syn1$ combination.

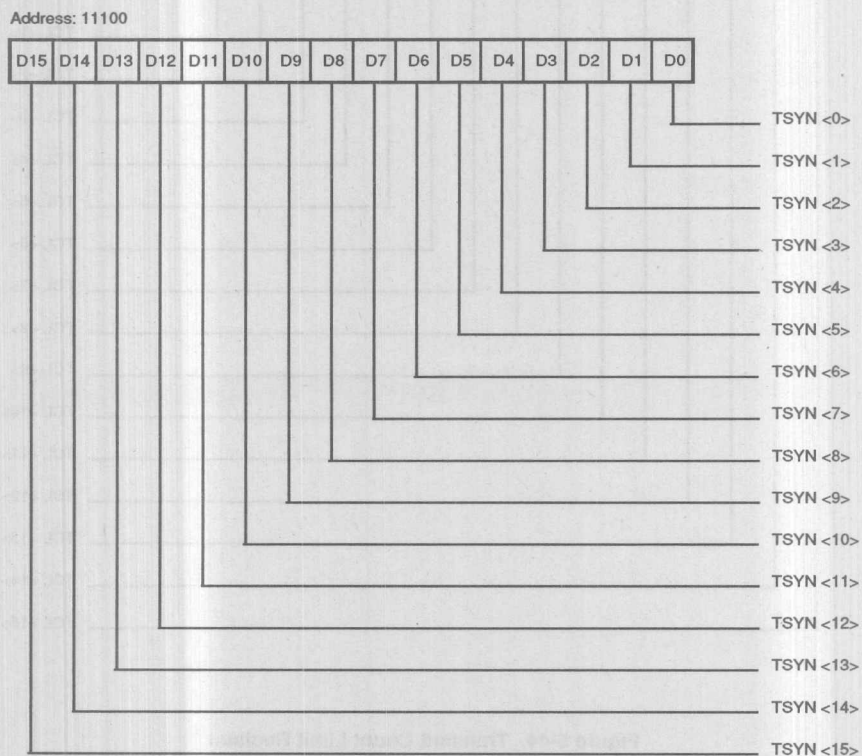


Figure 5-43. Transmit Sync Register

5.32 TRANSMIT COUNT LIMIT REGISTER

The Transmit Count Limit Register (TCLR) holds the starting count value for the transmit character counter (Figure 5-44).

The transmit character counting operation is disabled while this register contains all zeros. A non-zero value in this register indicates the number of bytes of data to be sent in this frame or message. The number in this register is the number of data bytes only; it does not include the number of bytes in the transmit status block, if any. The counting operation does not begin until after any transmit status block has been transferred.

Any transmit character counting operation in progress is unaffected by writing a new value to this register, even if the new value is zero, which disables the character counting operation. Writing a non-zero value to this register does not, in itself, enable the transmit character counting operation. Rather, the character counting operation is enabled or disabled and the transmit character counter is loaded either by the trigger transmit DMA command, the reload transmit character count command, the transmit FIFO purge command or loading the second word of a transmit status block.

The current count value may be read in the TCCR.

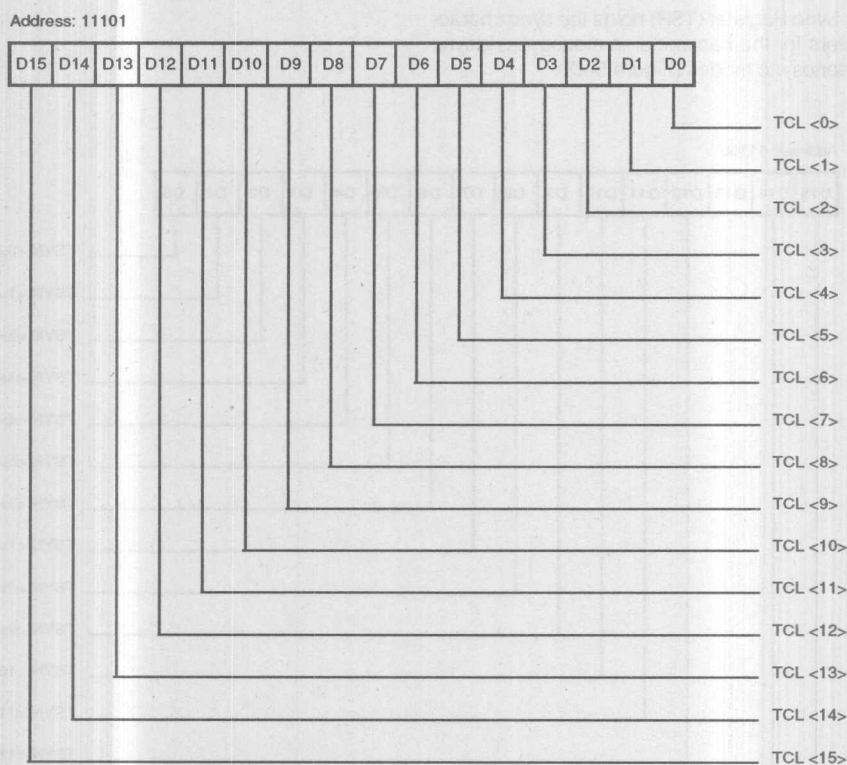


Figure 5-44. Transmit Count Limit Register

5.33 TRANSMIT CHARACTER COUNT REGISTER

The Transmit Character Count Register (TCCR) reports the current count in the transmit character counter (Figure 5-45).

The transmit character counter may be used in message or frame-oriented protocols to automatically determine the end of the message or frame. The transmit character counter is decremented by one for a byte and by two for a word, as data is written to the transmit FIFO. The byte that is written to the FIFO with a transmit character count of one is marked in the FIFO as the end-of-frame. When this last byte is written the transmit DMA request will be deasserted until this last byte is removed from the FIFO to ensure that the transmit status block for the following frame, if any, does not affect the current frame. Upon decrementing to a count of zero, DMA requests may be further inhibited until

a transmit DMA trigger command is issued, if programmed in the CCR.

In the case of a word transfer with a count of one, only the byte on AD0-7 is written to the FIFO and marked as the end-of-frame and the other byte is ignored. The byte marked as the end-of-frame in the FIFO causes the frame or message to be terminated with that byte. CRC may be transmitted following this byte if enabled with the CRC on EOF bit in the TMR. The frame or message is then terminated as programmed by the Tx Underrun Condition bit(s) in the CMR.

The character counting operation is enabled or disabled and the transmit character counter is loaded from the TCLR, either by the trigger transmit DMA, reload transmit character count or transmit FIFO purge command in the CCAR, or by loading the second word of a transmit status block.

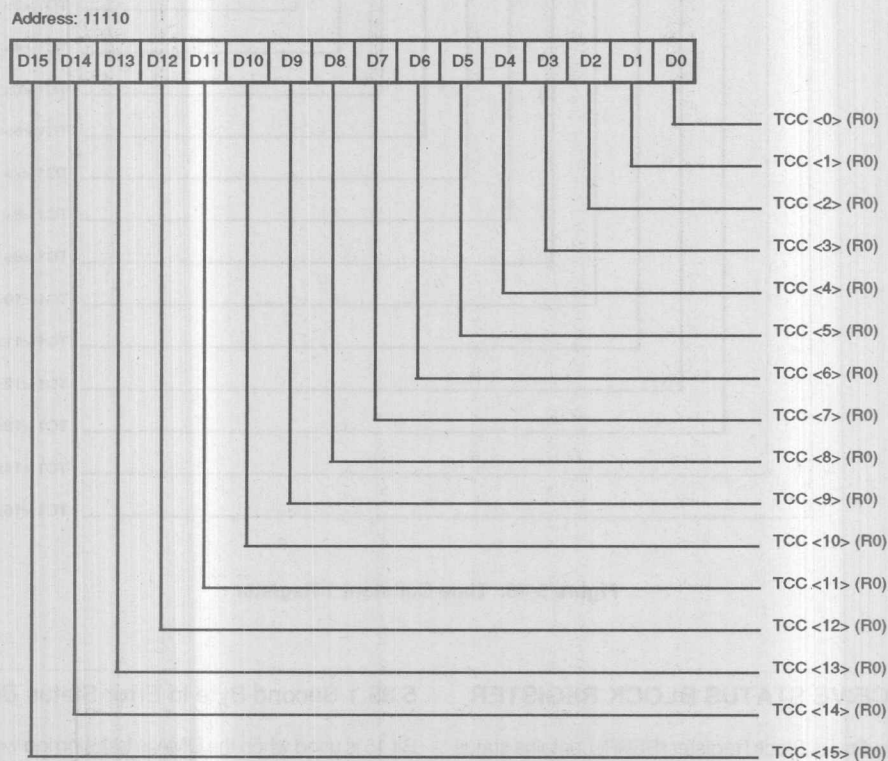


Figure 5-45. Transmit Character Count Register

5.34 TIME CONSTANT 1 REGISTER

The Time Constant 1 Register (TC1R) holds the time constant used by baud rate generator 1 (Figure 5-46).

The TC1R is a read/write register, but the value returned during a read depends on the state of the TC1R Read Count/TC control bit in the TCCR. If the TC1R Read Count/TC control bit in the TCCR is set to zero, the time constant is returned during the read; otherwise the current count in the counter is returned.

The counter in the baud rate generator automatically reloads the time constant when a count of zero is reached in continuous mode, and stops at the count of zero when operating in the single-cycle mode. The time constant may be loaded into the counter with a command in the CCAR.

The baud rate generator divides its input clock by the value of the time constant, plus one, to provide the baud rate generator output. The output of the baud rate generator is always a square wave.

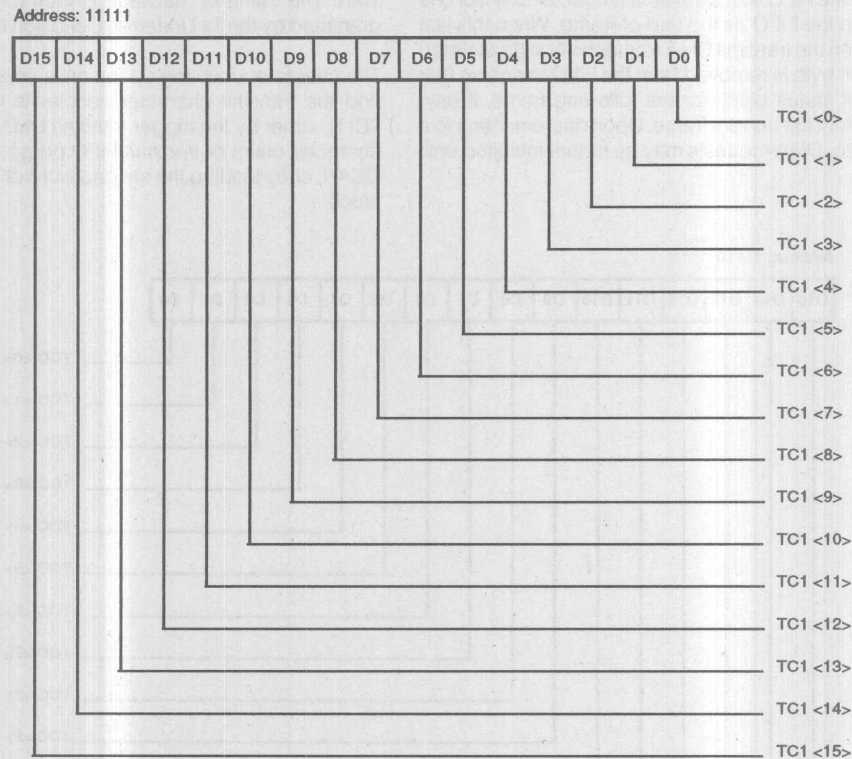


Figure 5-46. Time Constant 1 Register

5.35 RECEIVE STATUS BLOCK REGISTER

The Receive Status Block Register (RSBR) contains status information for the received message or frame that may be transferred to memory with the data under DMA control (Figure 5-47).

5.35.1 Second Byte in Error Status Bit

Bit 15 is used when the DMA is transferring words from the FIFO to mark the second byte received in the last word transferred by the DMA as the byte marked with a parity error, an overrun error, or the CV/EOT/EOF bit set to 1.

If this bit is set to 1, both bytes of the last word transferred to memory by the DMA contain valid data.

5.35.2 First Byte in Error Status Bit

Bit 14 is used when the DMA is transferring words from the FIFO to mark the first byte received in the last word transferred by the DMA as the byte marked with a parity error, an overrun error, or the CV/EOT/EOF bit set to 1.

If this bit is set to 1, only the first received byte of the last word transferred to memory by the DMA contains valid data.

5.35.3 Reserved Bits

Bits 13 and 12 are reserved and will always be read as 0.

5.35.4 Residue Code Status Field

Bits 11 through 9 report the number of valid data bits in the last byte of the received HDLC frame.

These three bits are used only when HDLC or HDLC Loop mode has been selected and are set to 000 in all other modes.

The residue code is independent of the number of bits per character selected for the receiver, and in all cases, the most significant bits of the last byte in the frame contain the valid data bits. The residue code is read-only.

Bit combination 000 indicates that the last byte in the frame contains eight valid data bits.

Bit combination 001 indicates that the last byte in the frame contains one valid data bit.

Bit combination 010 indicates that the last byte in the frame contains two valid data bits.

Bit combination 011 indicates that the last byte in the frame contains three valid data bits.

Address: XXXXX

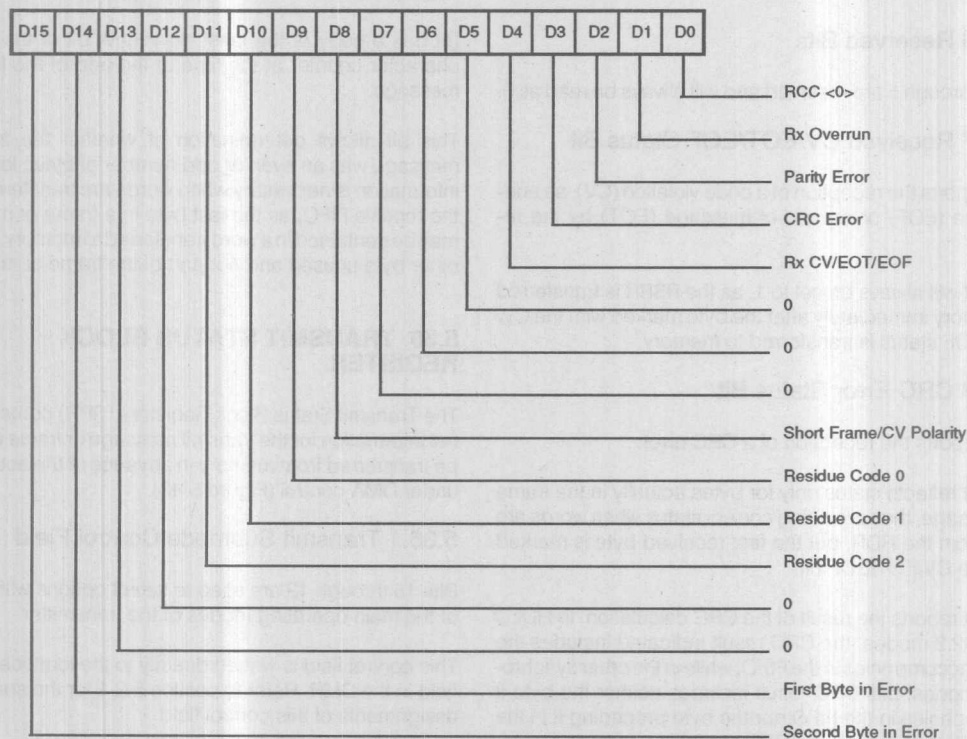


Figure 5-47. Receive Status Block Register

Bit combination 100 indicates that the last byte in the frame contains four valid data bits.

Bit combination 101 indicates that the last byte in the frame contains five valid data bits.

Bit combination 110 indicates that the last byte in the frame contains six valid data bits.

Bit combination 111 indicates that the last byte in the frame contains seven valid data bits.

5.35.5 Short Frame/CV Polarity Status Bit

Bit 8 reports the length status of the received HDLC frame or the polarity of a received code violation.

In the async with code violation mode, this bit reports the polarity of the received code violation pattern. Refer to Section 5.2 for the specific code violation waveforms and their polarity. In HDLC mode, a 1 in this bit indicates that the received frame was shorter than the minimum allowed, based on the lengths selected for the address and control fields in the CMR.

5.35.6 Reserved Bits

Bits 7 through 5 are reserved and will always be read as 0.

5.35.7 Received CV/EOT/EOF Status Bit

Bit 4 reports the reception of a code violation (CV), an end-of-frame (EOF) or an end-of-message (EOT) by the receiver.

This bit will always be set to 1, as the RSBR is transferred to memory immediately after the byte marked with the CV/EOT/EOF status is transferred to memory.

5.35.8 CRC Error Status Bit

Bit 3 reports the reception of a CRC error.

This bit reflects status only for bytes actually in the frame or message, thus providing correct status when words are read from the RDR, but the first received byte is marked with the CV/EOT/EOF bit.

This bit reports the result of the CRC calculation. In HDLC and 802.3 modes, the CRC result indicated includes the byte it accompanies in the FIFO, while in the other synchronous modes, this CRC result includes neither the byte it accompanies in the FIFO nor the byte preceding it in the FIFO. Thus, to check the CRC result through a particular byte, both that byte and the succeeding byte must be read from the FIFO before the CRC status is available.

5.35.9 Parity Error Status Bit

Bit 2 reports the parity error status of the receiver.

This bit reflects status only for bytes actually in the frame or message, thus providing correct status when words are read from the RDR, but the first received byte is marked with the CV/EOT/EOF bit.

5.35.10 Receive Overrun Status Bit

Bit 1 reports the overrun status of the receive FIFO.

This bit reflects status only for bytes actually in the frame or message, thus providing correct status when words are read from the RDR, but the first received byte is marked with the CV/EOT/EOF bit.

Once an overrun has occurred, no further writes to the FIFO are performed until a Receive FIFO Purge command is issued in the CCAR.

5.35.11 Receive Character Counter Bit 0 Status Bit

Bit 0 is a copy of the least significant bit of the receive character counter at the time of the end of the frame or message.

This bit allows determination of whether the frame or message was an even or odd number of bytes long. This information is necessary when words are transferred from the receive FIFO, as the last byte in a frame or message may be contained in a word transferred to memory, with the other byte unused and not part of the frame or message.

5.36 TRANSMIT STATUS BLOCK REGISTER

The Transmit Status Block Register (TSBR) contains control information for the transmit message or frame that may be transferred from memory in advance of the actual data under DMA control (Figure 5-48).

5.36.1 Transmit Submode Control Field

Bits 15 through 12 are used to select options within each of the main operating modes of the transmitter.

This control field is written directly to the identical control field in the CMR. Refer to section 5.2.1 for the specific bit assignments of this control field.

Bit combination 111 selects a character length of seven bits.

5.36.4 Reserved Bits

Bits 1 and 0 are reserved and should be 0.

5.37 BUS CONFIGURATION REGISTER

The Bus Configuration Register (BCR) contains control bits which tailor the bus interface to specific CPU interface requirements (Figure 5-49).

This register is accessed automatically by the first write to the device after a hardware reset, irrespective of the address presented to the device for that write. The configuration selected then applies until another hardware reset is performed.

5.37.1 Separate Address for 8-Bit Control Bit

Bit 15 is used to enable the separate address option in the case of an eight bit bus interface.

0 in this bit disables the separate address option for an eight bit bus. This bit must be written with 0 for a 16-bit bus interface.

1 in this bit enables the separate address option for an eight bit bus. In this case AD8 is the U//L signal, AD13-9 are Address4-0 respectively, AD14 must be tied Low and AD15 must be tied High.

5.37.2 Tri-State All Pins Control Bit

Bit 14 is used during device testing to force all pins to the high-impedance state.

This bit should be used only for testing purposes; always write a 0 to this bit.

0 in this bit allows normal pin function.

1 in this bit places all pins in the high-impedance state. Only a hardware reset may be used to exit this state.

5.37.3 Reserved Bits

Bits 13 through 8 are reserved.

5.37.4 WRSTBT Timing Adjust Control Bit

Bits 7 through 5 are used to adjust the width of the internal write strobe signal.

These bits are reserved for parametric measurements and are not guaranteed to be present in future versions of the device.

Bit combination 000 disables the width adjustment circuitry for the internal write strobe signal.

Bit combination 001 adds 2.5nS to the width of the internal write strobe signal.

Bit combination 010 adds 5nS to the width of the internal write strobe signal.

Bit combination 011 adds 7.5nS to the width of the internal write strobe signal.

Bit combination 100 disables the width adjustment circuitry for the internal write strobe signal.

Bit combination 101 subtracts 2.5nS from the width of the internal write strobe signal.

Bit combination 110 subtracts 5nS from the width of the internal write strobe signal.

Bit combination 111 subtracts 7.5nS from the width of the internal write strobe signal.

5.37.5 Output /WRSTB on /IVACK Control Bit

Bit 4 is used to enable the routing of the internal write strobe signal to the /IVACK pin.

This bit is reserved for parametric measurements and is not guaranteed to be present in future versions of the device.

0 in this bit disables the routing of the internal write strobe signal to the /IVACK pin.

1 in this bit enables the routing of the internal write strobe signal to the /IVACK pin for parametric measurements.

5.37.6 Bus is /RDSTB and /WRSTB Control Bit

Bit 3 is used to configure the bus to provide read strobe and write strobe directly.

This bit is reserved for parametric measurements and is not guaranteed to be present in future versions of the device.

0 in this bit allows normal bus operation.

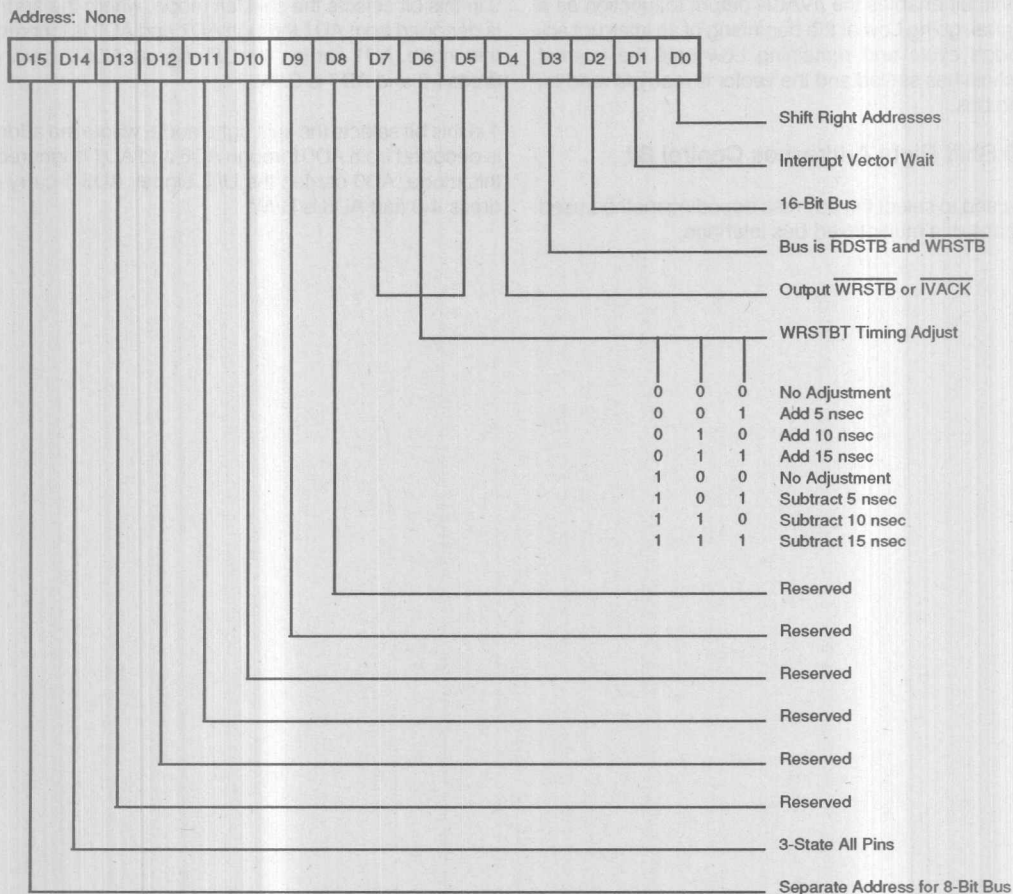


Figure 5-49. Bus Configuration Register

1 in this bit configures the $\overline{\text{RD}}$ signal to provide the internal read strobe signal directly and the $\overline{\text{WR}}$ signal to provide the internal write strobe signal directly.

5.37.7 16-Bit Bus Control Bit

Bit 2 is used to distinguish between an eight bit bus and a 16-bit bus.

0 in this bit selects eight bit bus operation for the device.

1 in this bit selects 16-bit bus operation for the device.

5.37.8 Interrupt Vector Wait Control Bit

Bit 1 is used to select the type of acknowledge signal present on the $\overline{\text{IVACK}}$ pin during an interrupt acknowledge cycle.

The CPU must not terminate the interrupt acknowledge cycle until the device has released this signal, indicating that the internal daisy-chain has settled.

A 0 in this bit enables the $\overline{\text{IVACK}}$ output to function as a Ready signal, going Low during an interrupt acknowledge cycle when the internal daisy-chain has settled and the vector is ready to read on the data bus.

A 1 in this bit enables the /IVACK output to function as a Wait signal, going Low at the beginning of an interrupt acknowledge cycle and remaining Low until the internal daisy-chain has settled and the vector is ready to read on the data bus.

5.37.9 Shift Right Addresses Control Bit

Bit 0 is used to select the address decoding method used in the case of a multiplexed bus interface.

0 in this bit selects the shift left mode, where the address is decoded from AD1 through AD7 and AD0 is ignored. In this mode, AD1 carries the U/L signal, AD6-2 carry Address 4-0 and AD7 is B/W.

1 in this bit selects the shift right mode, where the address is decoded from AD0 through AD6 and AD7 is ignored. In this mode, AD0 carries the U/L signal, AD5-1 carry Address 4-0 and AD6 is B/W.



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CHAPTER 6

TEST MODES

6.1 INTRODUCTION

The USC has incorporated a unique feature which will allow the user a special access to internal registers for testing purposes. The user will be able to trace the data through the USC in order to debug and/or optimize his software.

The nodes and registers are accessed through the Test Register Access field bits D4 through D0 in the Test Mode Control Register (TMCR, Figure 6-1) at address 00111. The data for the register selections is available in the Test

Mode Data Register (TMDR, Figures 6-2 through 6-33) at address 00110. The specific data bit assignments for each mode in the test registers are shown in the accompanying figures.

Note: The access time of the TMDR is approximately three times the access time of the other registers in the channel. Keep this in mind when designing hardware to support this feature.

6.2 REGISTER DEFINITIONS

The following 32 figures show the various test modes displayed by the Test Mode Control Register (TMCR) at address 00111.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
-----	-----	-----	-----	-----	-----	----	----	----	----	----	----	----	----	----	----



TMCR Contents: 00000

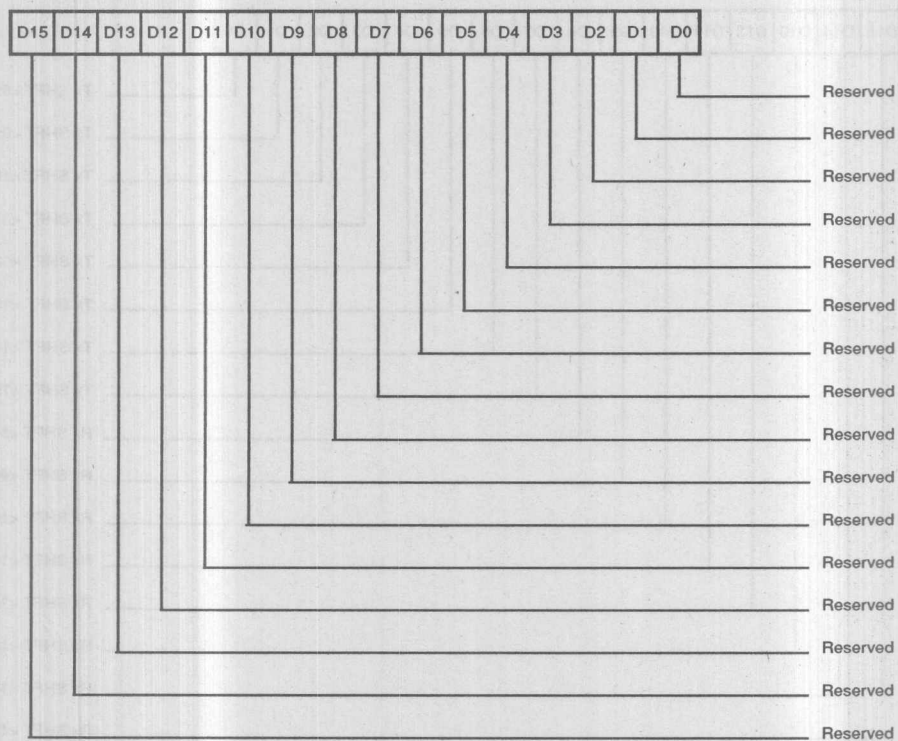


Figure 6-2. Test Mode Data Register (Reserved)

TMCR Contents: 00001

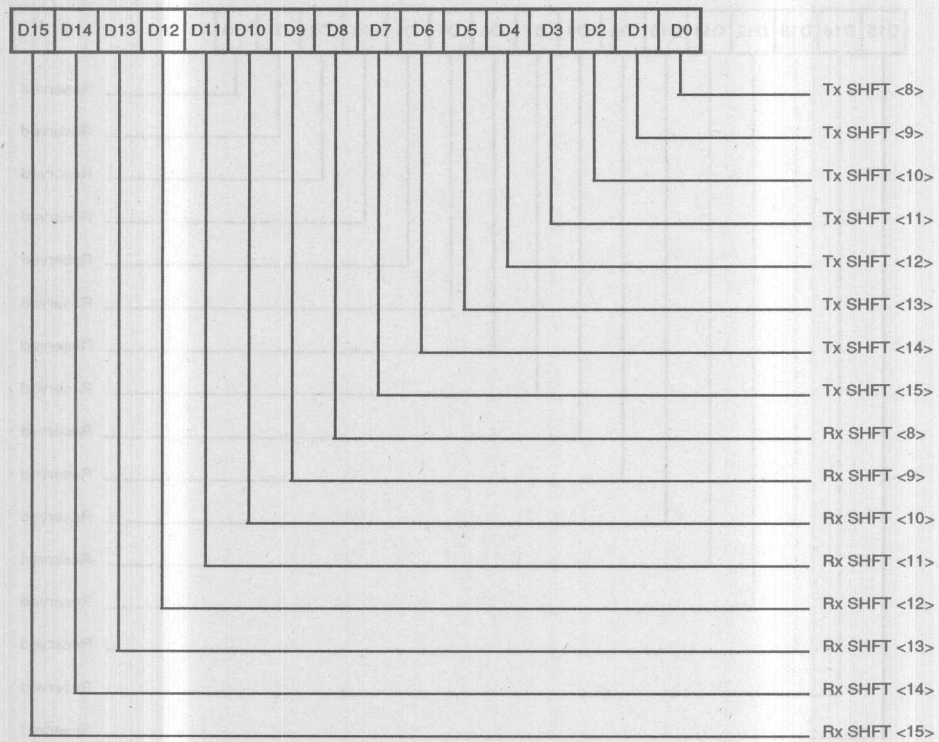


Figure 6-3. Test Mode Data Register (High Byte of Shifters)

TMCR Contents: 00010

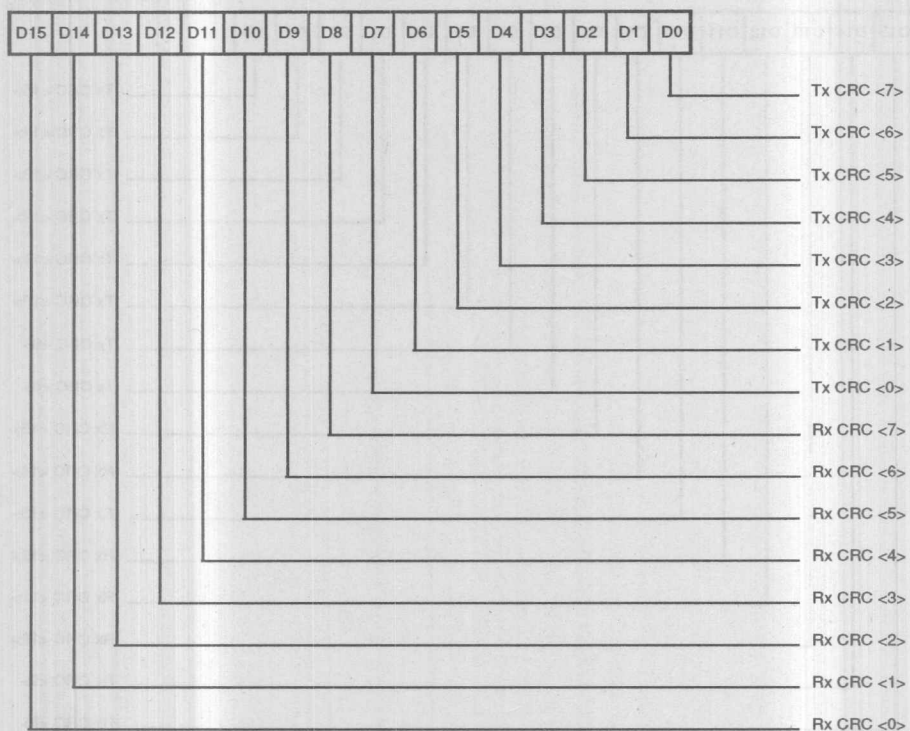


Figure 6-4. Test Mode Data Register (CRC byte 0)

TMCR Contents: 00011

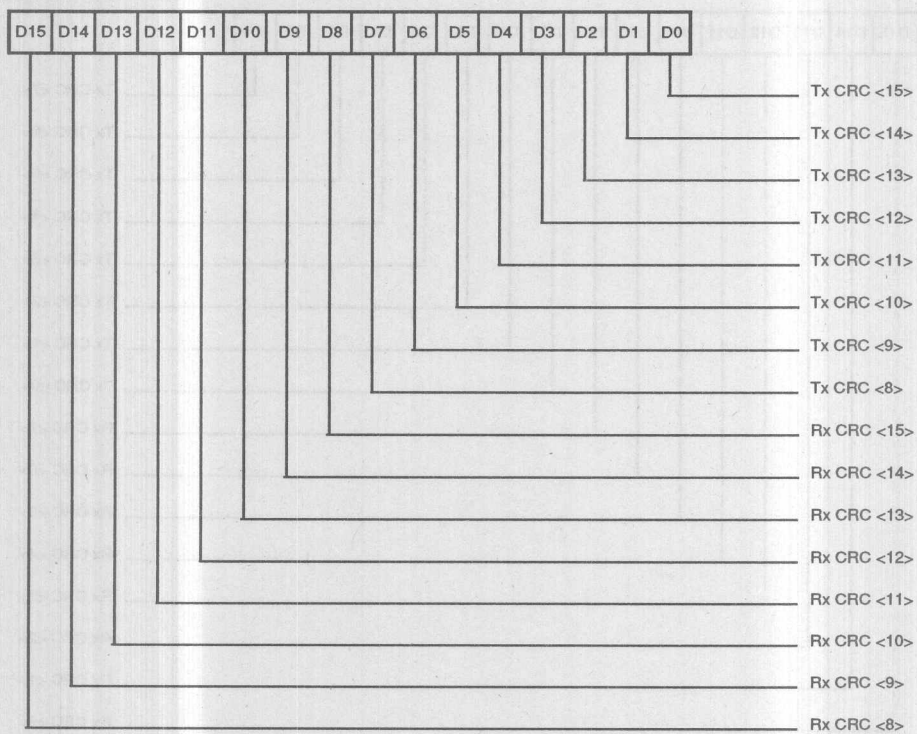


Figure 6-5. Test Mode Data Register (CRC byte 1)

TMCR Contents: 00100

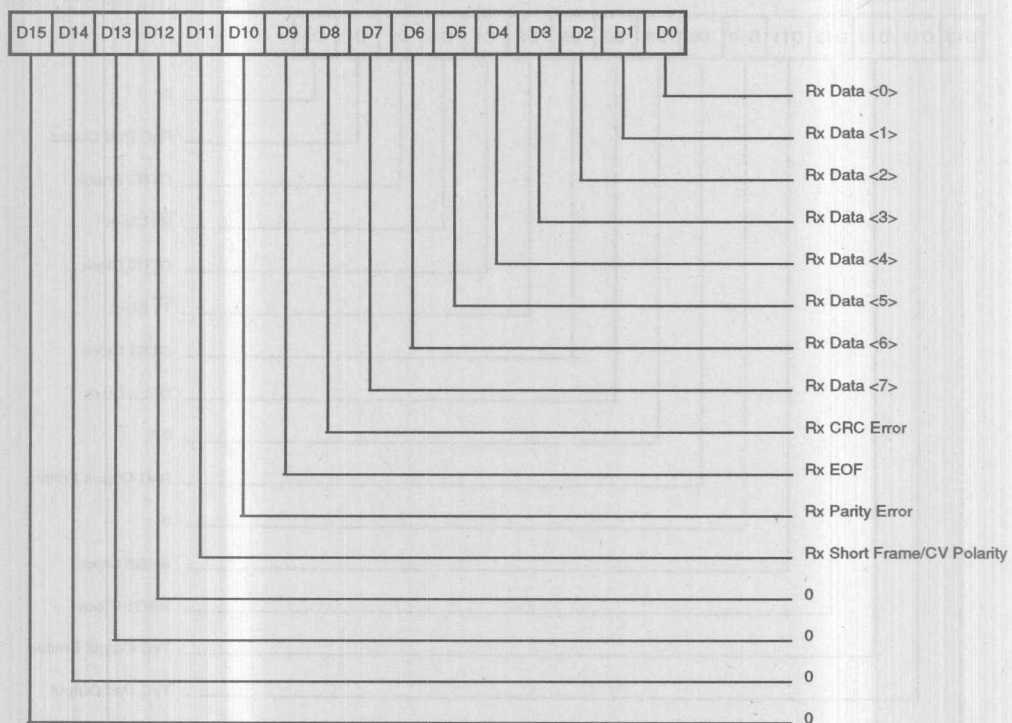


Figure 6-6. Test Mode Data Register (Rx FIFO)

TMCR Contents: 00101

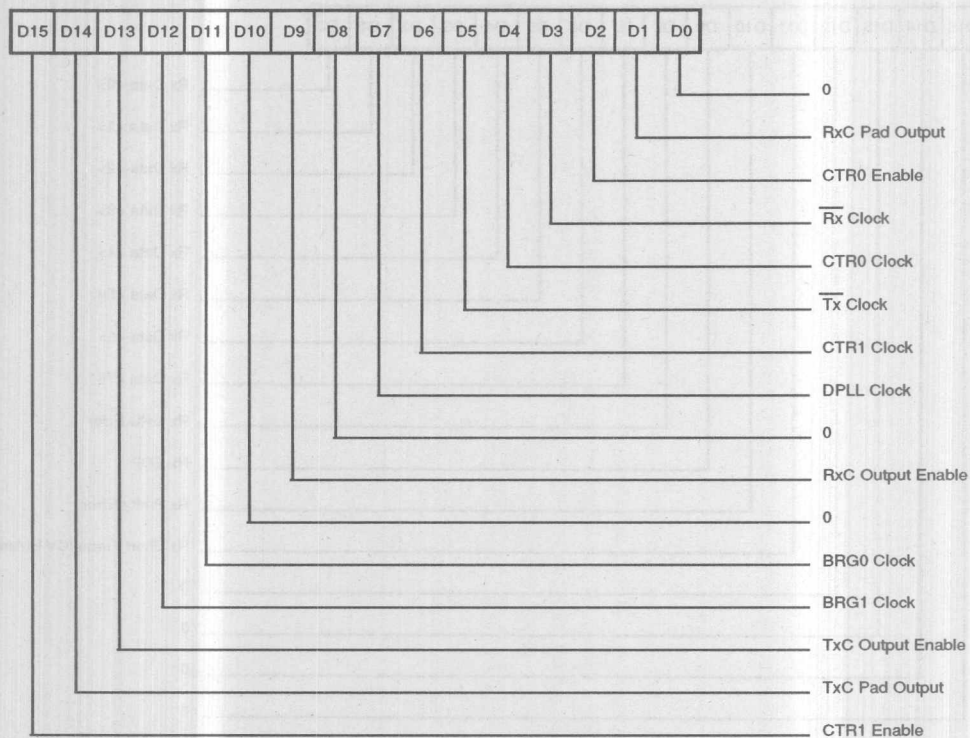


Figure 6-7. Test Mode Data Register (Clock Mux Outputs)

TMCR Contents: 00110

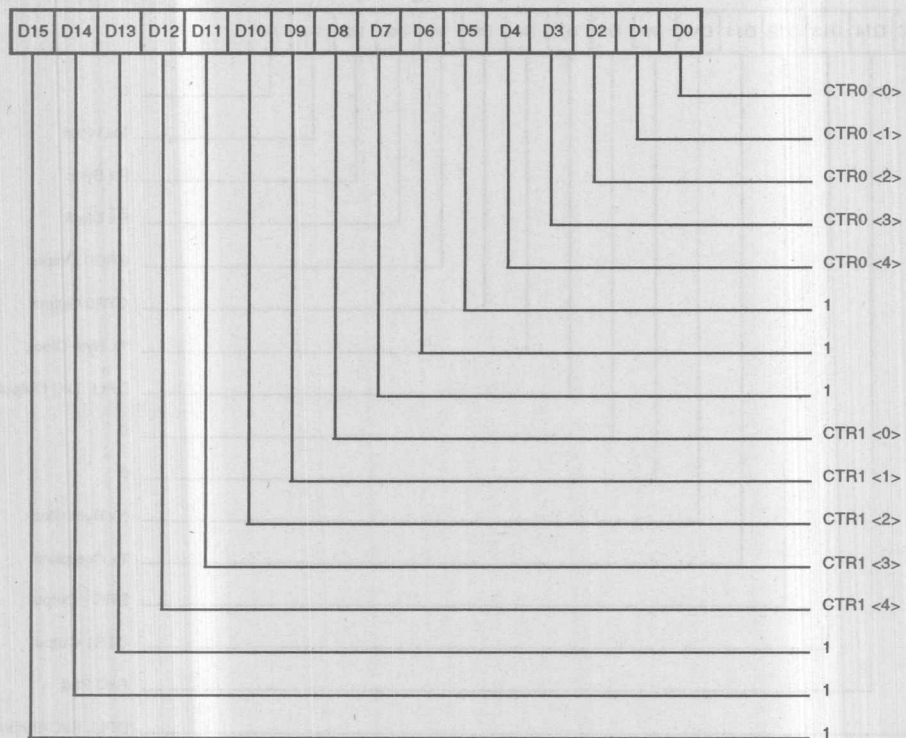


Figure 6-8. Test Mode Data Register (CTR1 and CTR0)

TMCR Contents: 00111

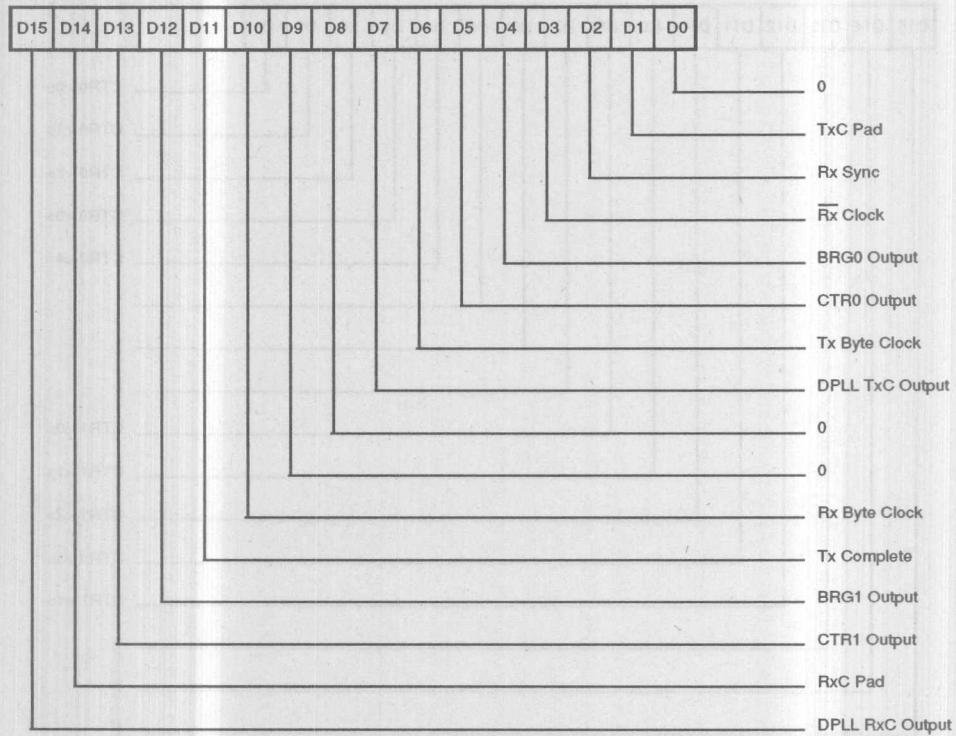


Figure 6-9. Test Mode Data Register (Clock Mux Inputs)

TMCR Contents: 01000

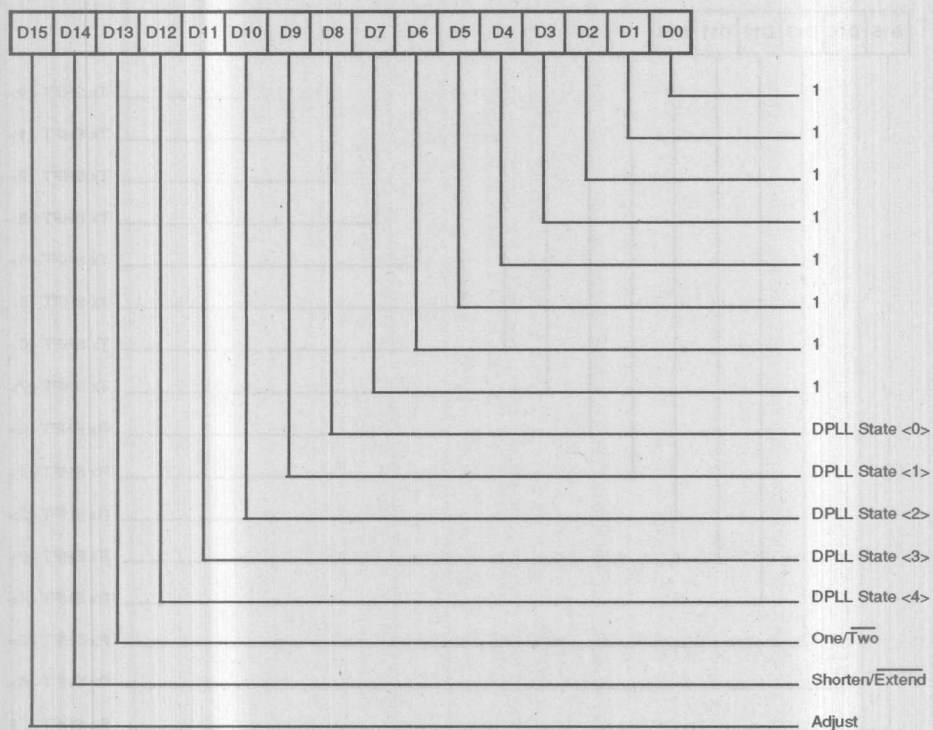


Figure 6-10. Test Mode Data Register (DPLL State)

TMCR Contents: 01001

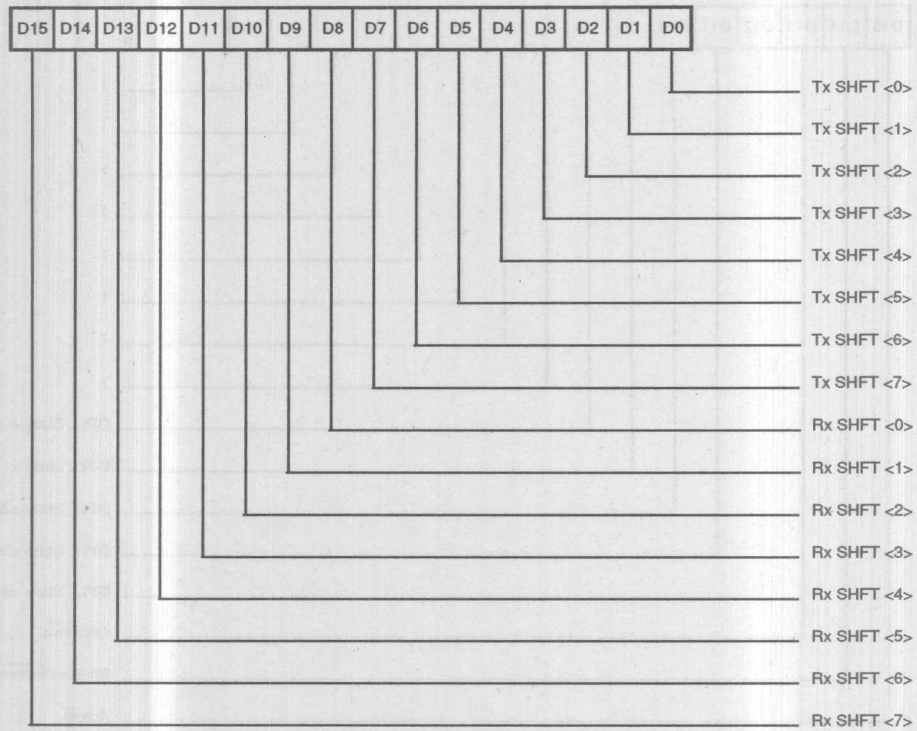


Figure 6-11. Test Mode Data Register (Low Byte of Shifters)

TMCR Contents: 01010

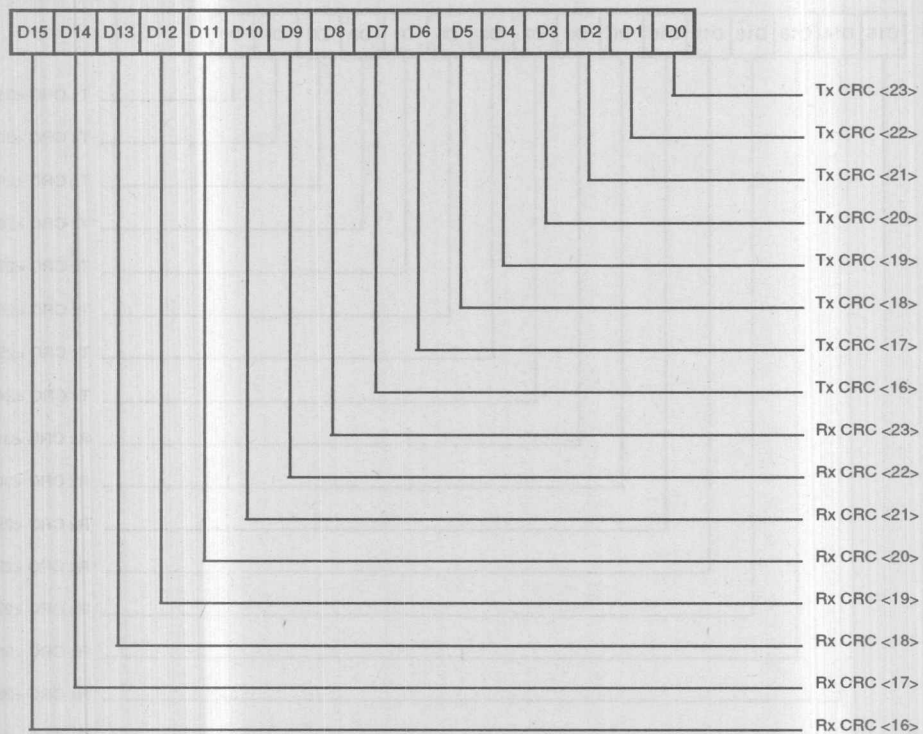


Figure 6-12. Test Mode Data Register (CRC Byte 2)

TMCR Contents: 01011

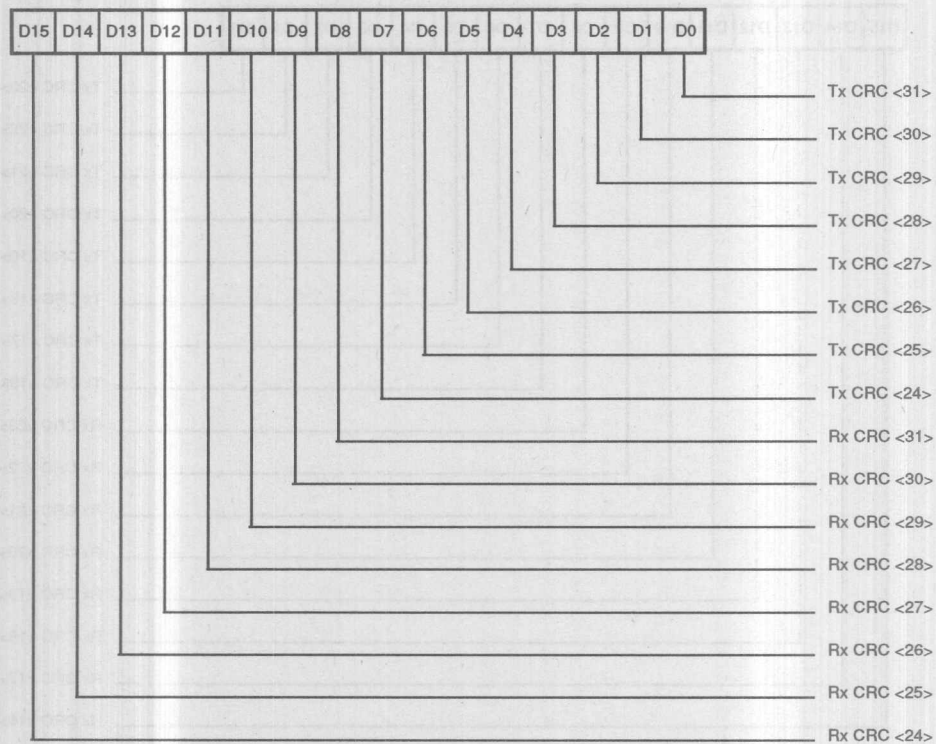


Figure 6-13. Test Mode Data Register (CRC Byte 3)

TMCR Contents: 01100

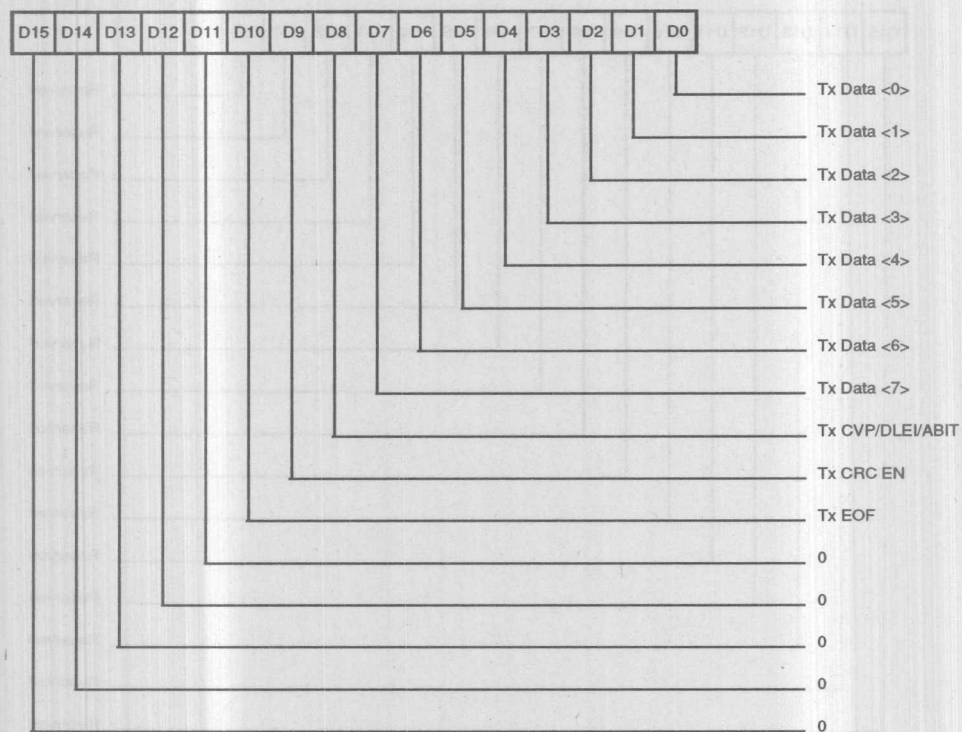


Figure 6-14. Test Mode Data Register (Tx FIFO)

TMCR Contents: 01101

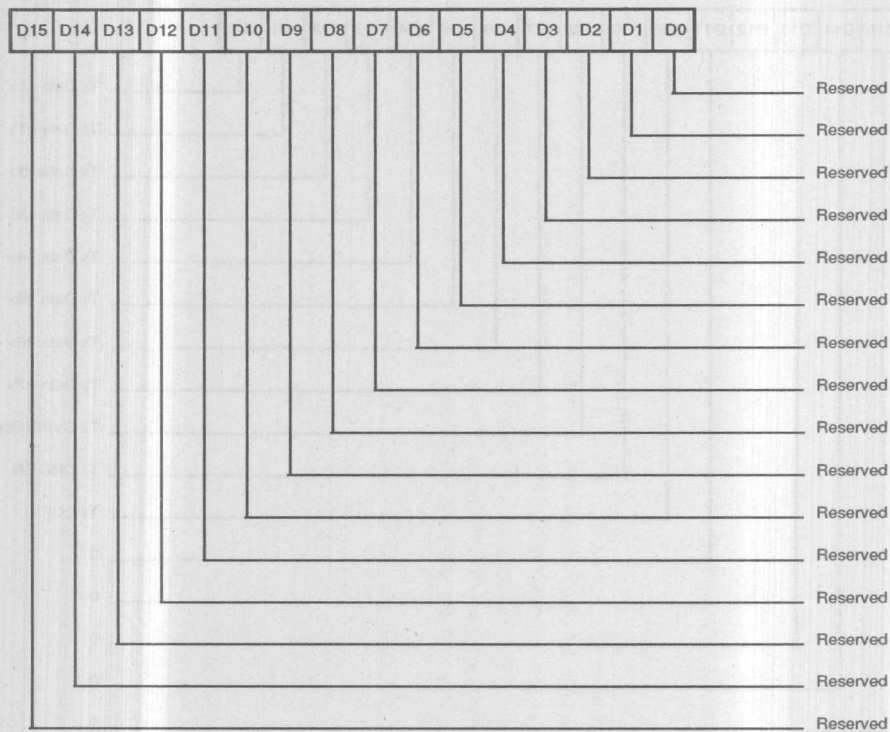


Figure 6-15. Test Mode Data Register (Reserved)

TMCR Contents: 01110

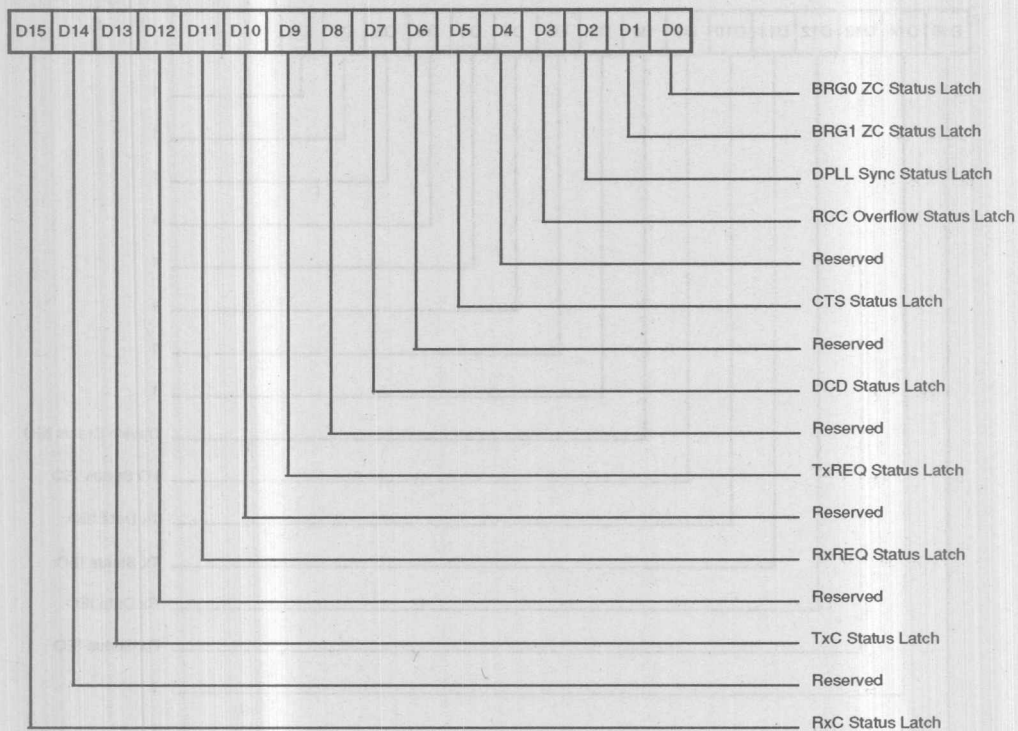


Figure 6-16. Test Mode Data Register (I/O and Device Status)

TMCR Contents: 01111

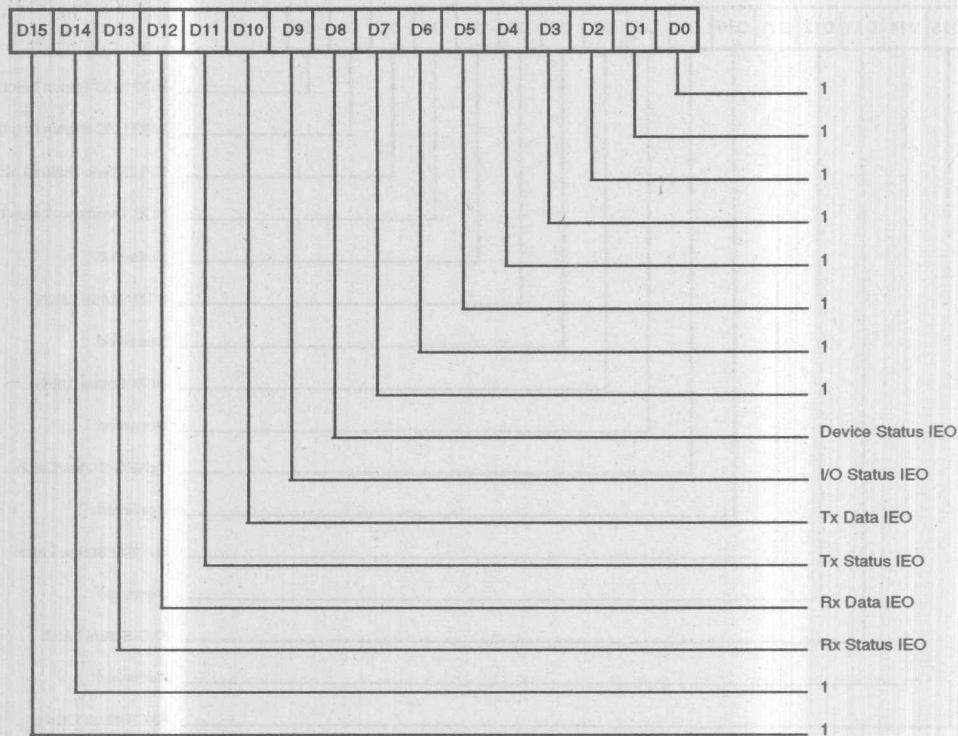


Figure 6-17. Test Mode Data Register (Interrupt Daisy-Chain)

TMCr Contents: 10000

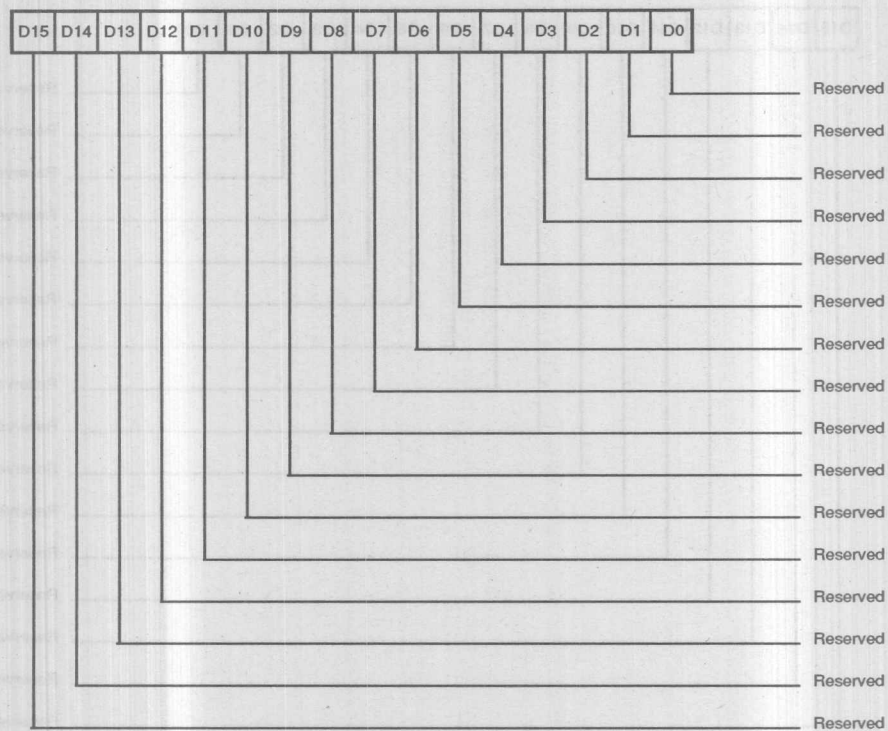


Figure 6-18. Test Mode Data Register (Reserved)

TMCR Contents: 10001

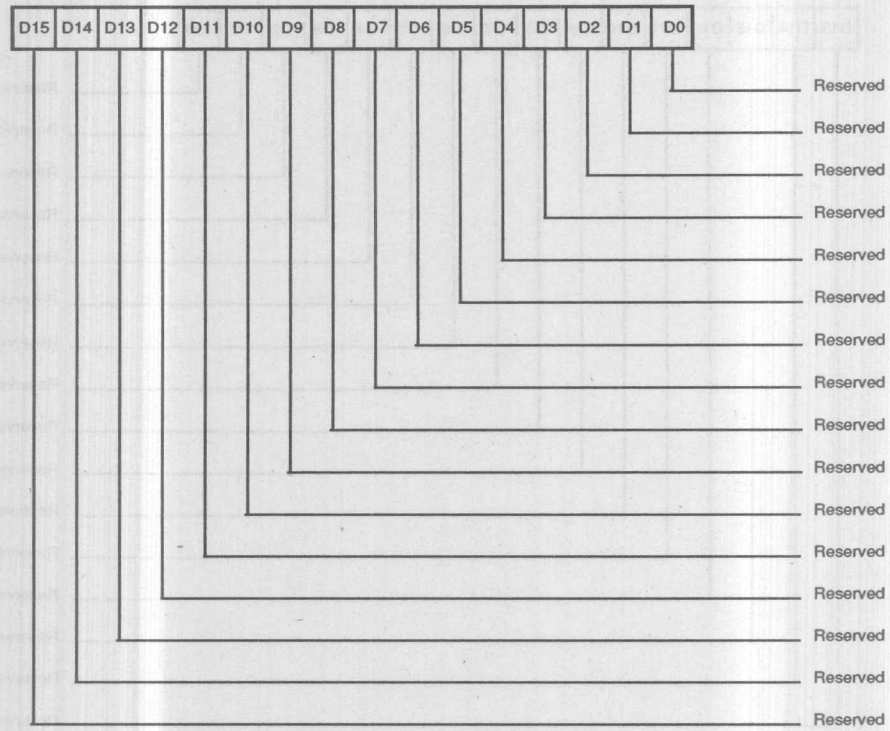


Figure 6-19. Test Mode Data Register (Reserved)

TMCR Contents: 10010

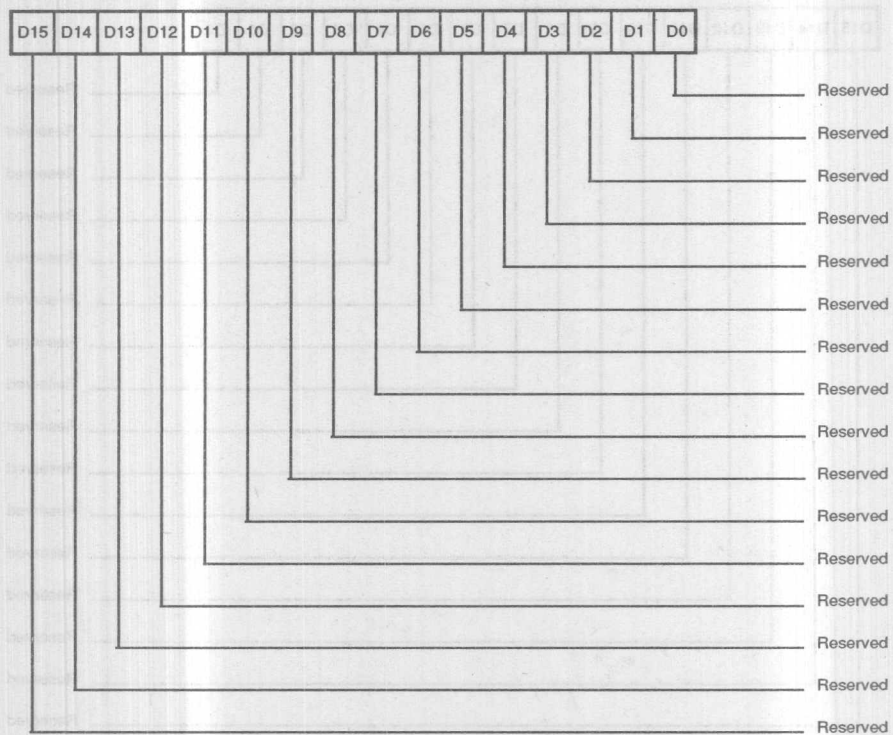


Figure 6-20. Test Mode Data Register (Reserved)

TMCR Contents: 10011

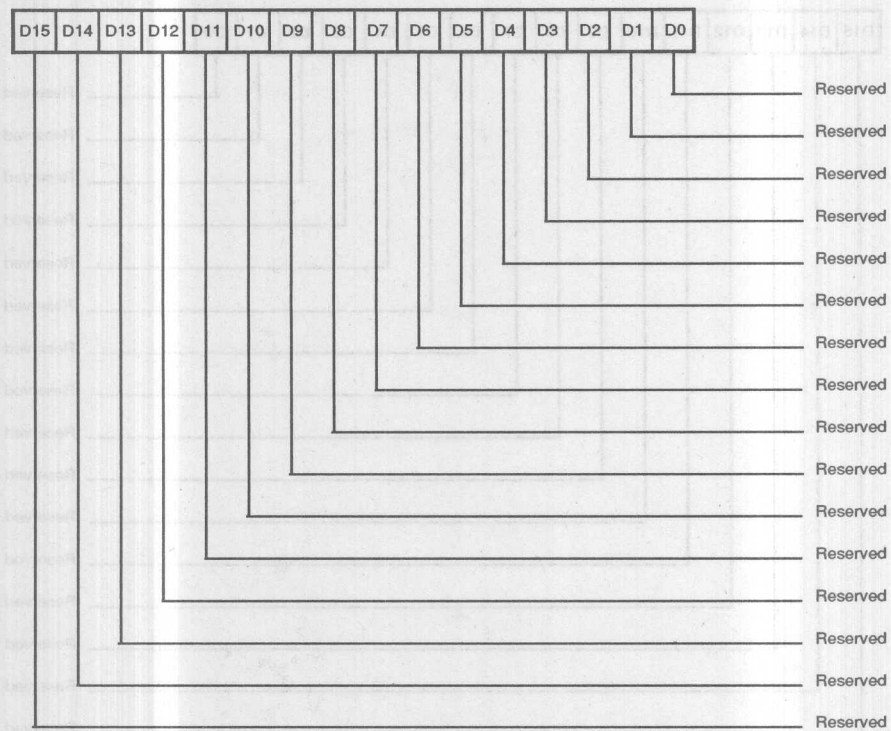


Figure 6-21. Test Mode Data Register (Reserved)

TMCr Contents: 10100

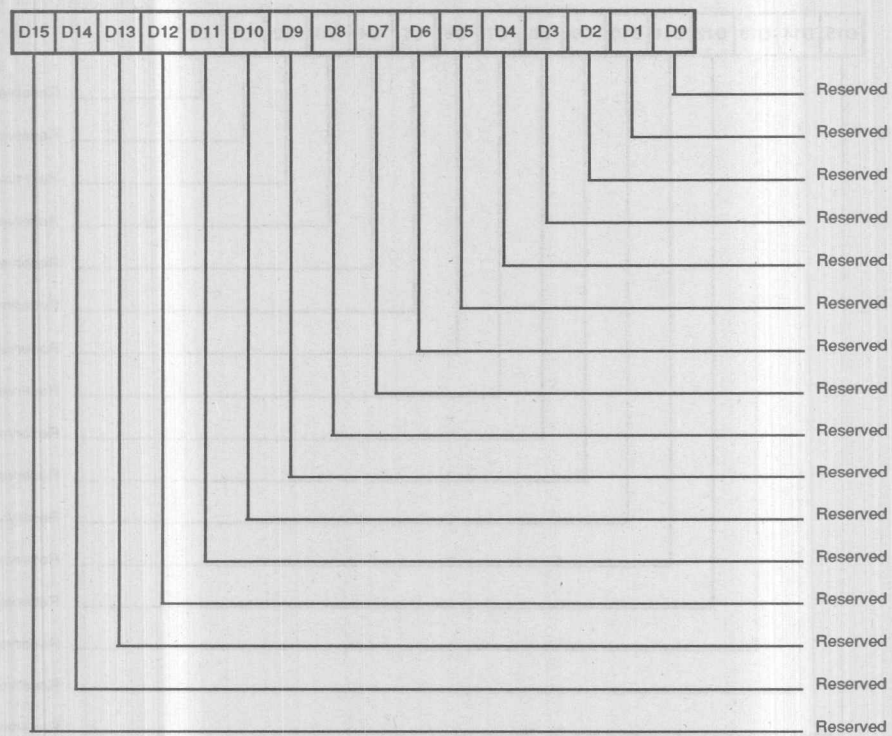


Figure 6-22. Test Mode Data Register (Reserved)

TMCR Contents: 10101

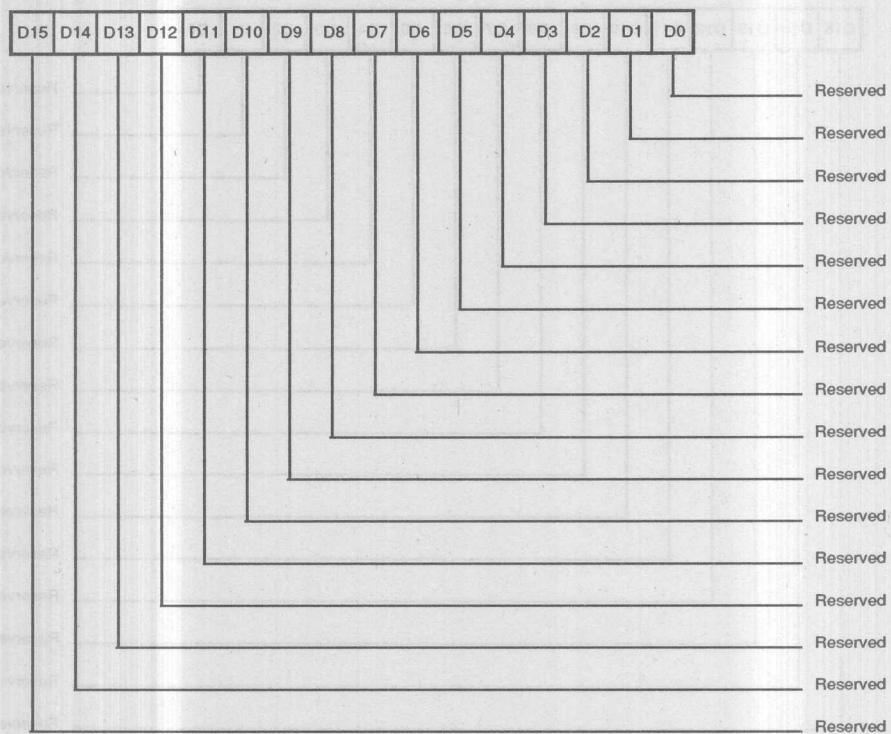


Figure 6-23. Test Mode Data Register (Reserved)

TMCR Contents: 10110

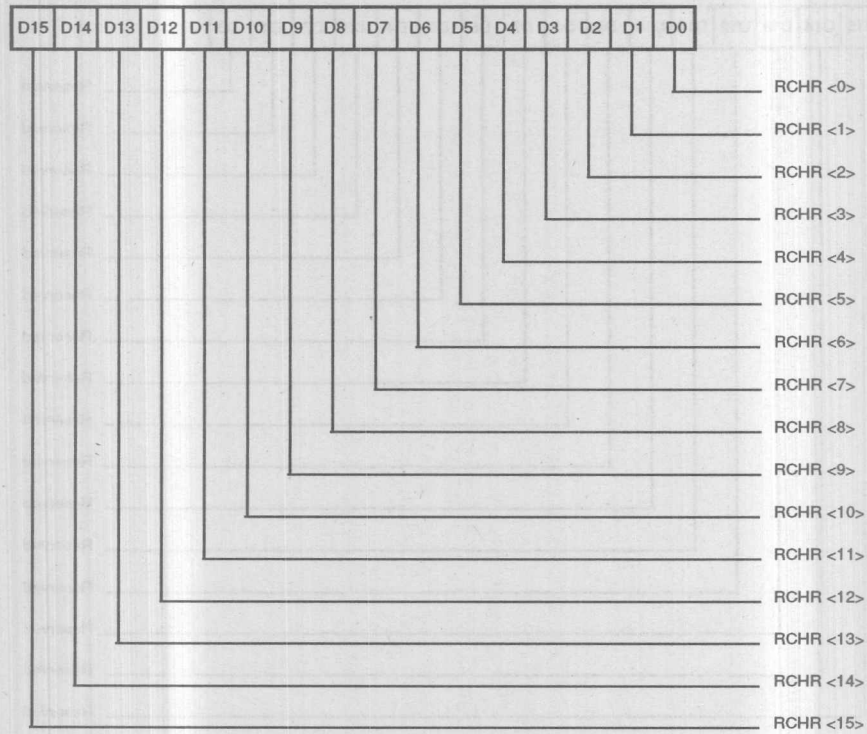


Figure 6-24. Test Mode Data Register (Rx Count Holding Register)

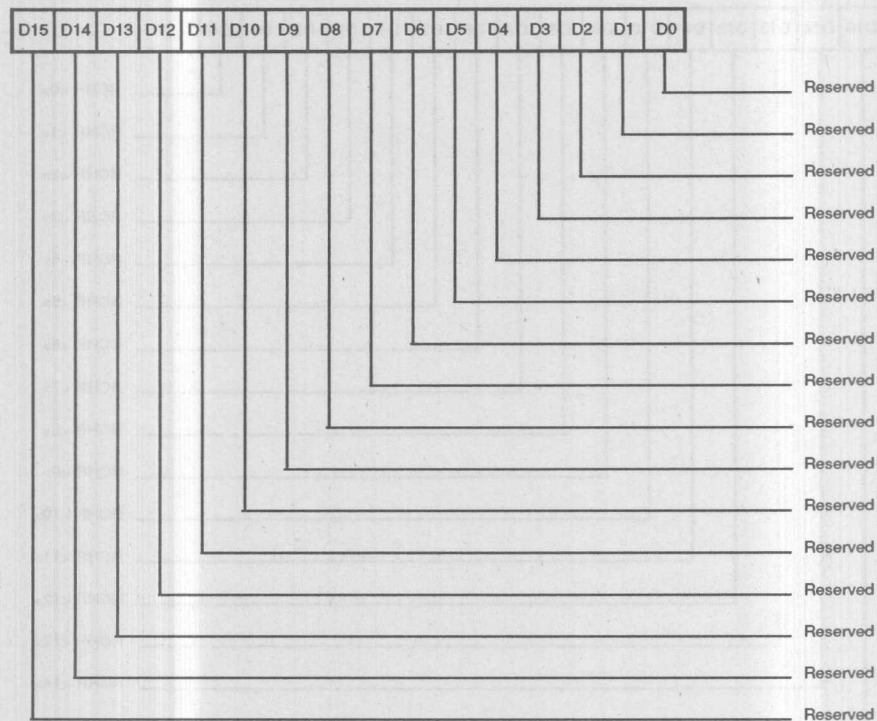


Figure 6-25. Test Mode Data Register (Reserved)

TMCR Contents: 11000

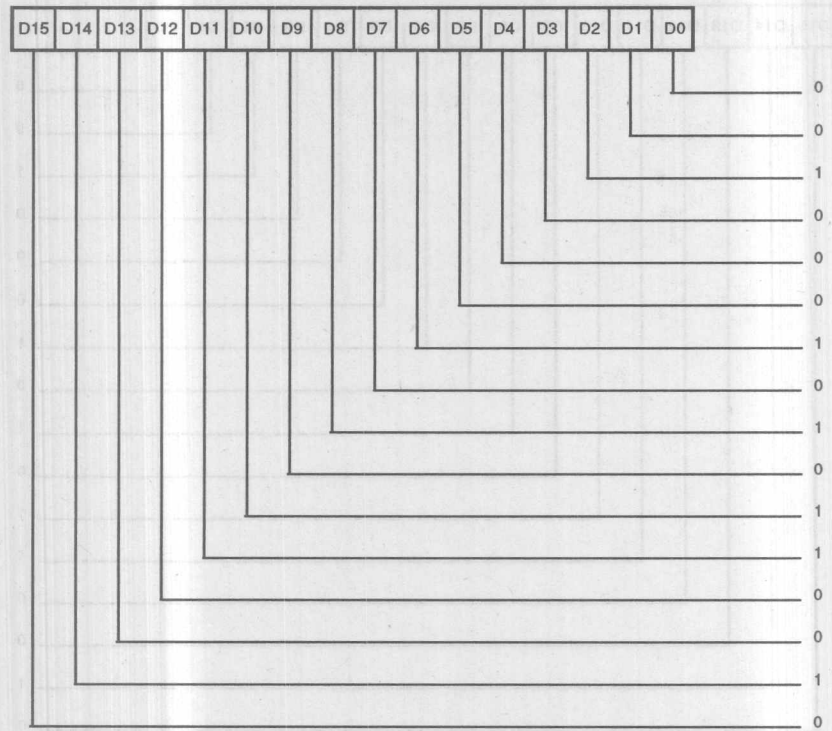


Figure 6-26. Test Mode Data Register (Reserved)

TMCR Contents: 11001

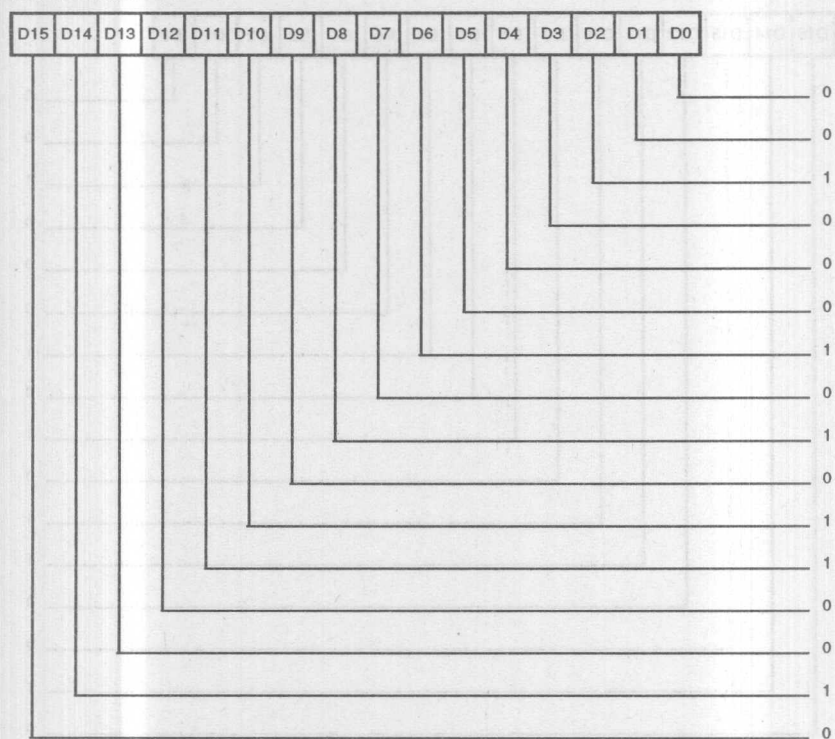


Figure 6-27. Test Mode Data Register (Reserved)

TMCR Contents: 11010

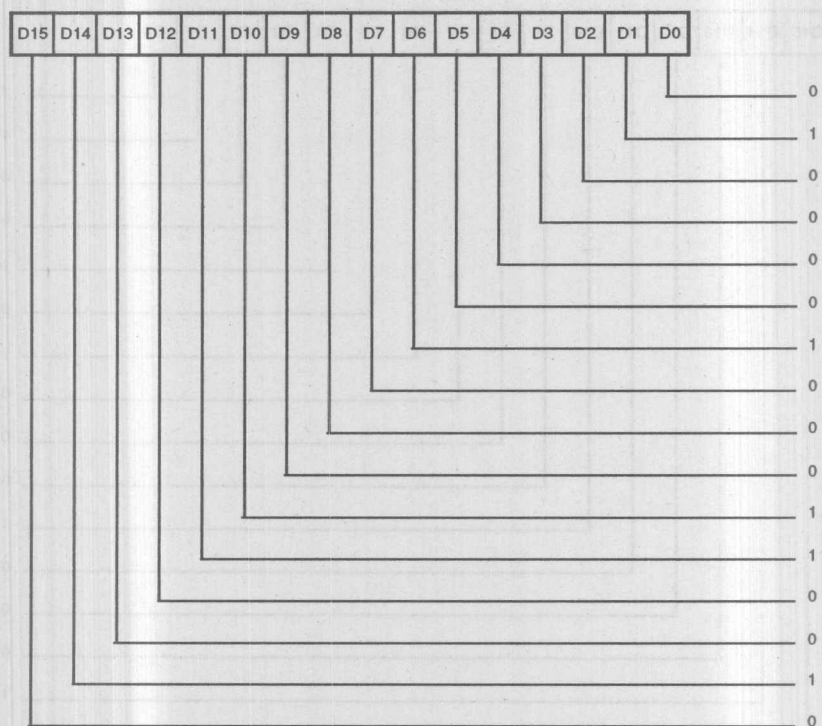


Figure 6-28. Test Mode Data Register (Reserved)

TMCR Contents: 11011

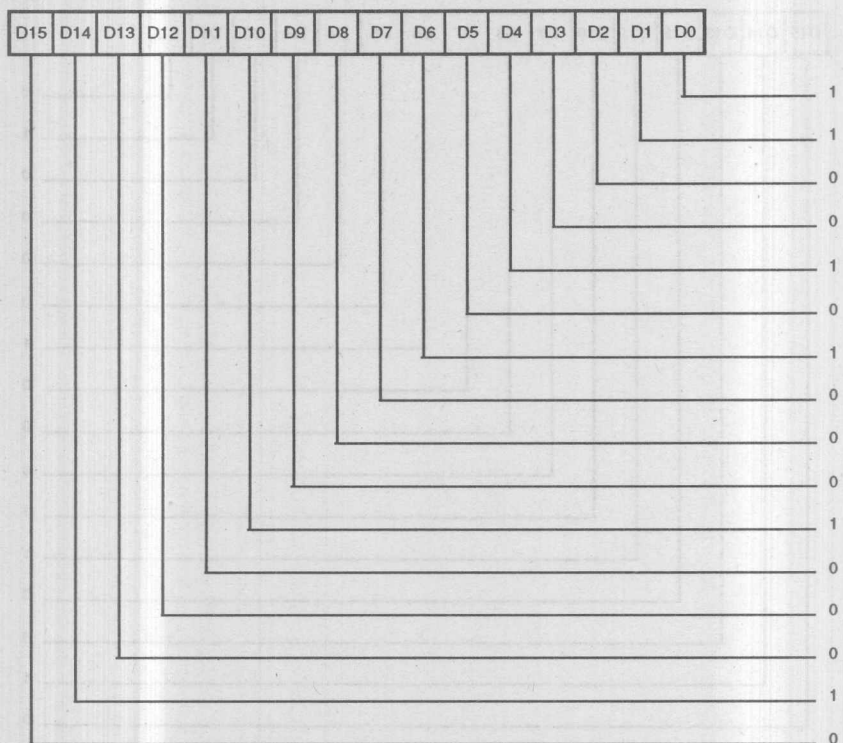


Figure 6-29. Test Mode Data Register (Reserved)

TMCR Contents: 11100

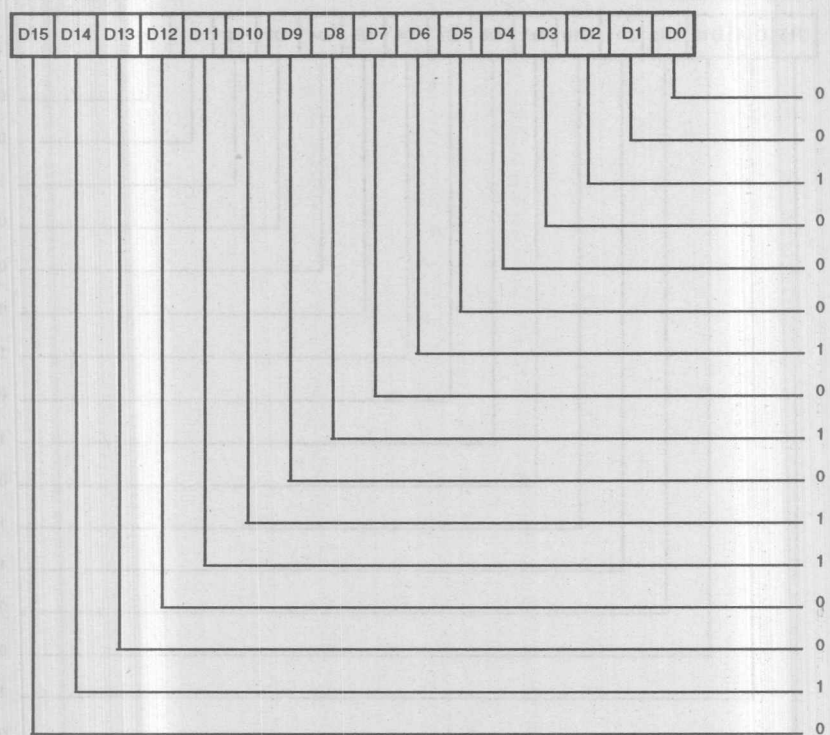


Figure 6-30. Test Mode Data Register (Reserved)

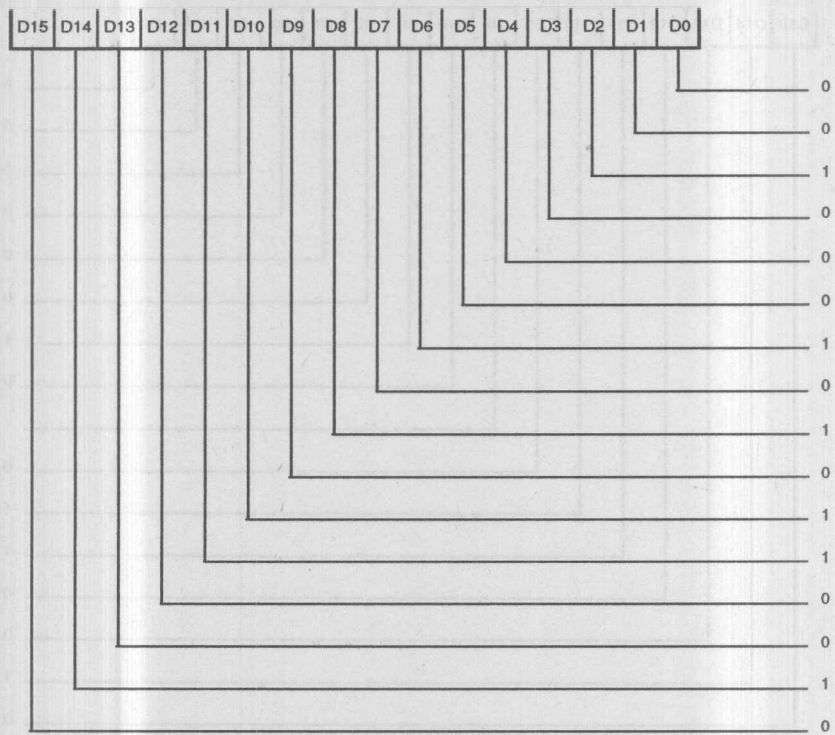


Figure 6-31. Test Mode Data Register (Reserved)

TMCR Contents: 11110

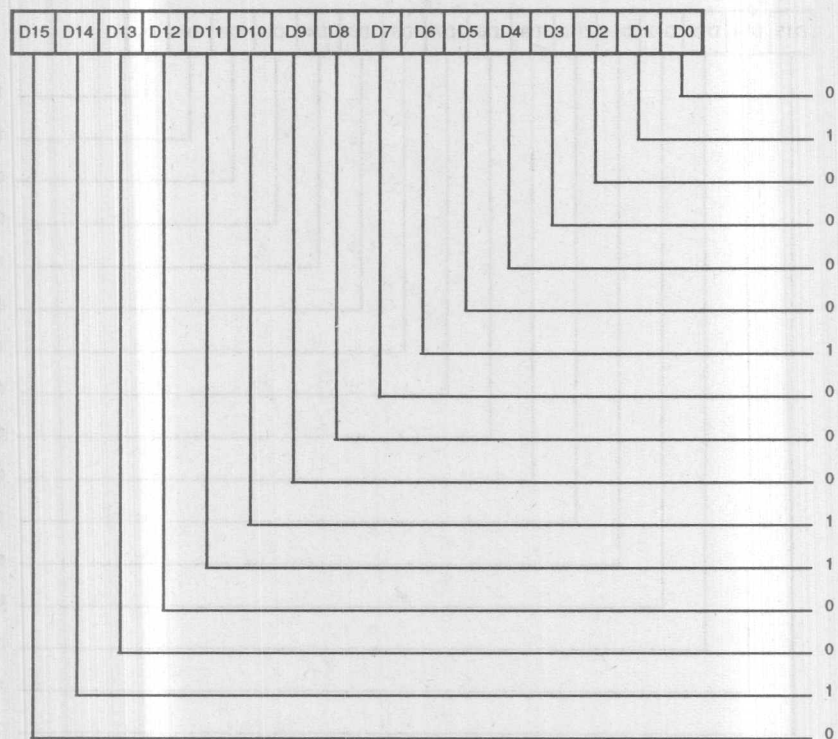


Figure 6-32. Test Mode Data Register (Reserved)

TMCR Contents: 11111

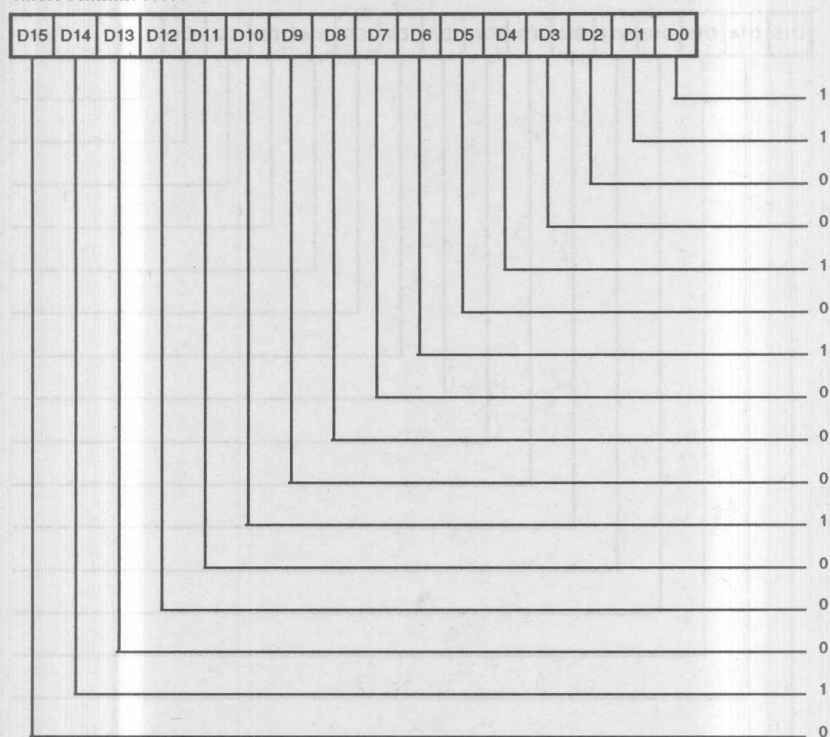


Figure 6-33. Test Mode Data Register (Reserved)



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APPENDIX A

UNIVERSAL SERIAL CONTROLLER

Table A-1. ASYNC (Polled)

Rx		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Async Mode	CMR													0	0	0	0
16x Data Rate	CMR											0	0				
Clock Source = BRG0	CMCR														1	0	0
Bits/Char = 8-bits	RMR													0	0	0	
Even Parity	RMR										0	0	1				
NRZ	RMR	0	0	0													
Tx		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Async Mode	CMR					0	0	0	0								
16x Data Rate	CMR				0	0											
2 Stop Bits	CMR	0	1														
Clock Source - BRG0	CMCR														1	0	0
Bits/Char = 8-Bits	TMR												0	0	0		
Even Parity	TMR									0	0	1					
NRZ	TMR	0	0	0													
BRG0		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Continuous Cycle	HCR								1	0							
Clock Source = RxC	CMCR																
Time Count =	TCOR	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Enables		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Enable BRG0	HCR															1	
Enable Rx																	
Without Auto Enable	RMR														1	0	
Enable Tx																	
Without Auto Enable	RMR														1	0	
Polled		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
No Interrupts	TCR	0															

Legend: Blank = 0
X = User's Value

Rx		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bisync Mode	CMR													0	1	0	1
Sync Char is 8-Bits	CMR												0				
Sync Char is	RSR																
Clock Source = DPLL Out	CMCR														0	1	1
8 Bits/Char	RMR													0	0	1	
Even Parity	RMR									0	0	1					
CRC is CRC-32	RMR				1	1											
Preset CRC to 0's	RMR						0										
Data Encoding is																	
Biphase-Mark	RMR	1	0	0													
Max. # of Data/Frame	RCLR																

Tx		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Bisync Mode	CMR					0	1	0	1								
8 Bit Sync Char	CMR				0												
Preamble is 8 Bit	CCR					0	0										
Preamble is Alt 1 & 0	CCR							1	0								
Transmit Underrun																	
Action is CRC/Syn/Syn1	CMR	1	1														
Sync Char is	TSR																
Clock Source is CTRO	CMCR											1	1	0			
8 Bits/Char	TMR												0	0	1		
Even Parity	TMR									1	0	0					
CRC is CRC-32	TMR				1	1											
Preset CRC to 0's	TMR				0												
Data Encoding is																	
Biphase-Mark	TMR	1	0	0													
Max. # of Data/Frame	TCLR																

DPLL		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Clock Source is TxC	CMCR									1	1						
DPLL Clock Rate = 16x	HCR					0	1										
DPLL Sync Edge is	CLSR							0	0								
DPLL Mode is																	
Biphase-Mark	HCR							1	0								

Enables		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Enable RxCRC	RMR							1									
Enable Rx																	
With Auto Enable	RMR														1	1	
Enable TxCRC	TMR							1									
Enable Tx																	
With Auto Enable	TMR														1	1	

Table A-2. SYNC Modes - BISYNC (Continued)

CTRO		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Clock Source is TxC	CMCR			1	1												
Clock Rate is 16x	HCR	0	1														
Int		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Int. Sources																	
Device	ICR																0
I/O Status	ICR															0	
Tx Data	ICR														0		
Tx Status	ICR													0			
Rx Data	ICR												0				
Rx Status	ICR											0					
Enable Status																	
Info. In Vector	ICR				1												
Int. Vector is	IVR									X	X	X	X	X	X	X	X
All Int. Sources																	
Encode Vector	ICR					0	0	0									
Provide Vector																	
During Int. Ack.	ICR			1													
Disable Lower																	
Daisy-Chain	ICR		1														
Rx Int.																	
Parity	RICR														1		
FIFO Overrun	RICR															1	
Status Int. on Bytes	RICR													0			
Rx Break/Abort	RICR											1					
Exit Hunt Int.	RICR								1								
Tx Int.																	
CRC Sent	TICR													1			
Abort Sent	TICR											1					
Wait for RxDMA	CCR											1					
Wait for TxDMA	CCR			1													

Table A-3. SYNC Modes - HDLC

Rx		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HDLC Mode	CMR													0	1	1	0
Logical Control Field Address Search is	CMR								1								
1 Byte + Control	CMR										1	1	0				
Station Address is	RSR	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Clock = DPLL Out	CMCR														0	1	1
8-Bits/Char	RMR												0	0	1		
No Parity	RMR								0	0	0						
CRC-32	RMR				1	1											
Preset CRC to All 1's	RMR						1										
Data Encoding is																	
Biphase-Space	RMR	1	0	1													
Max. # of Data/Frame	HDLC																
Tx		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
HDLC Mode	RMR					0	1	1	0								
Last Char Length (EOF) is 8-Bits	CCSR												0	0	0		
Transmit Underrun Action is CRC & Flags	CMR	1	1														
Preamble Length is 16-Bits	CCR					0	1										
Preamble Pattern is 1's and 0's	CCR							1	0								
Normal Line is Shared 0's	CMR				1												
Clock Source is CTR0	CMCR											1	1	0			
8-Bits/Char	TMR												1	1	1		
No Parity	TMR									0	0	0					
CRC-32	TMR				1	1											
Preset CRC to All 1's	TMR						1										
Data Encoding is																	
Biphase-Space	TMR	1	0	1													
Max. # of Data/Frame	TCLR																
CTR0		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Clock Source is TxC	CMCR									1	1						
DPLL Clock Rate = 16x	HCR					0	1										
DPLL Sync Edge is	CLSR							0	0								
DPLL Mode is																	
Biphase-Space	HCR							1	0								

Table A-3. SYNC Modes - HDLC (Continued)

Enables																			
Enable Rx CRC	RMR																		
Enable Rx																			
With Auto Enable																	1	1	
Enable Tx CRC	TMR																		
Enable Tx																			
With Auto Enable	TMR																1	1	
Int		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0		
Int Sources																			
Device	ICR																	0	
I/O Status	ICR																0		
Tx Data	ICR															0			
Tx Status	ICR														0				
Rx Data	ICR													0					
Rx Status	ICR												0						
Encode Status																			
Info. in Vector	ICR					1													
Int. Vector is	IVR										X	X	X	X	X	X	X	X	
All Int. Sources																			
Encode Vector	ICR						0	0	0										
Provide Vector																			
During Int. Ack.	ICR					1													
Disable Lower																			
Daisy-Chain	ICR					1													
Rx Int.																			
Parity	RICR															1			
FIFO Overrun	RICR																1		
Status Int. on Bytes	RICR														0				
Rx Break/Abort	RICR												1						
Exit Hunt Int.	RICR										1								
Tx Int.																			
CRC Sent	TICR														1				
Abort Sent	TICR										1								
Wait for Rx DMA	CCR										1								
Wait for Tx DMA	CCR					1													

